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Digital Camera Controller

STK1262B

Product Sheet V1.2

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1. Product Overview:

The STK1262B is a high performance, high integration single chip digital-still-video and live-video camera controller. The STK1262B can act as a high performance tethered camera, a high quality digital still camera or a high bandwidth digital video recorder all in one set of hardware and software. The high-speed architecture, high quality image processor and motion JPEG compression/decompression engine create the best bandwidth utilization path for video camera systems. The STK1262B is capable of outputting excellent quality 30 frame-per-second VGA images, from CMOS sensors through its interface. The STK1262B is also capable of storing JPEG compressed pictures on most popular nonvolatile memory or mini-storage cards. Other auxiliary features such as CSTN LCD interface, recording and playback, programmable user interface logic and power management are all integrated into a single chip. The Direct-Memory-Access logic that moves data between the storage device and memory buffer enables the STK1262B to perform as a digital video recording device.

The flexible architecture of the STK1262B enables it to support various applications such as digital still camera, video mail camera, video-conferencing camera, surveillance camera, Web camera, wireless camera, toy camera, toy camcorder and digital video recorder.

2. Product Features:

Dual Mode, High Quality Digital Still Camera plus PC Camera functions

- Support 2MP image sensors at capture mode(
- Support 640x480 (VGA) CMOS sensors up to 20 fps （AVI capture）, (30fps PC camera) at display or capture mode
- Also support CIF/QVGA, QCIF resolution CMOS sensors at 30 fps

JPEG Compression/Decompression Engine

- Baseline JPEG with Support for YCrCb 4:1:1 and 4:2:2 sampling in three component images
- Loadable quantization table to enhance picture quality and compression ratio
- Integrated downscale for decompressed images

Image Enhancement Engine

- Proprietary color interpolation filter to create missing color components
- Programmable Gamma correction table
- Support for auto white balancing and auto exposure
- Support for sensor color correction
- Advanced edge enhancement and color noise removal processing

Sensor Interface

- Seamless interface with most CMOS Image Sensor chips
- Supports VGA, CIF/QVGA and QCIF resolution sensor

Embedded Microcontroller

- Turbo8032 compatible micro-controller
- 8KB of zero wait state local SRAM (programmable code or data)

- Arithmetic engine for 32-bit operations

Memory Sub-System

- SDRAM up to 4MB, x16 external bus, support for degraded SDRAM
- DMA controller for fast storage data transfers
- ROM/NOR FLASH interface up to 2MB, x8 data width
- SPI serial Flash Interface
- Supports up to 4 SDRAM banks to reduce page break latency

Host Interface

- Fully compatible with full speed USB 1.1 Spec
- Supports USB Control, Interrupt, Bulk and Isochronous pipes:
  Automatic adjustable alternate setting to fit bandwidth budget
- 22-bit power-on strapping register for USB vender/product ID and enumeration

LCD Interface

- 256 colors overlay with 4-bit alpha blending channel
- Supports Solomon ST7636 controller CSTN panels (6-6-6 mode) Tianma and others
- Supports 1.1",1.33",1.5" CSTN Panel
- TN display with external controller

General Purpose Input/Output Interface

- 22 general purpose input/output ports for user interface and inter-component communication
- Interface with status LCD panel controller
- Supports Iris control
- Supports SCR flash bulb control
- Keyboard controller – two wire remote keyboard support

Miscellaneous Circuit

- Automatic TV detection comparator
- Battery-low voltage detector (8 levels)

Power management

- 1.8V core, 3.3V Input/Output Power Supply Voltage(±10% tolerance)
- Dynamic power management, independent module clock frequency setting and gating
- Low power consumption (250mA total system average during 5MP snapshot processing)

Software and Development System

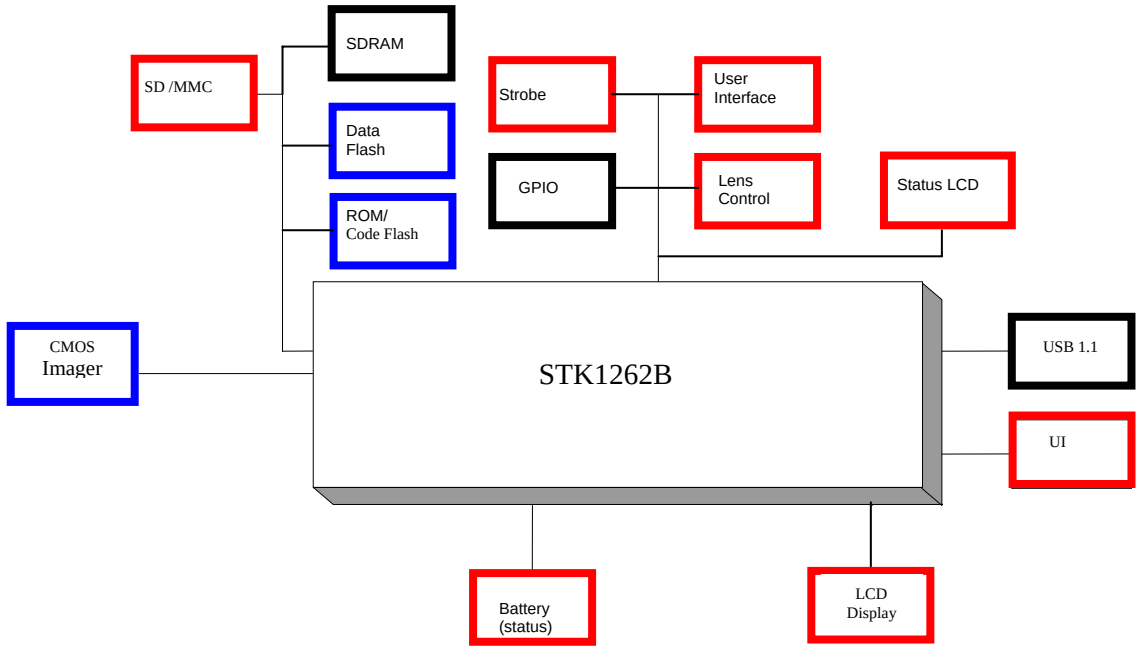
- Supports MS-Windows driver for Win98, Win2000, WinME, WinXP,VISTA
- TWAIN driver
- WIA driver
- Turbo-8032 firmware
- Reference development AP
- Reference development hardware platform

Package

- 128-pin LQFP

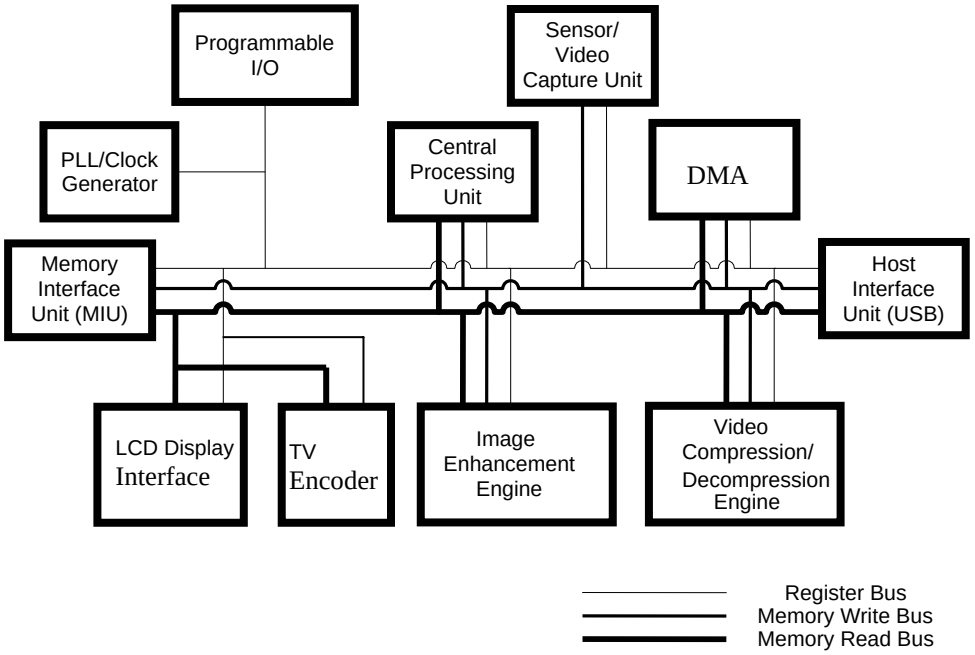
3. Block Diagrams:

3.1 System Block Diagram



STK1262B System Block Diagram

3.2 Internal Block Diagram



1262B Internal Block Diagram

4. Pin List:

STK1262B				
Pin	Pad Names	PU/PD	I/O	Comment
	GPIO			
63	GPIO0<0>	PU	I/O	Also serves as internal timer1 output.
60	GPIO0<7>		I/O	Also serves as the input for 8051 int1_n.
58	GPIO1<0>	PU	I/O	Also serves as output port for VCLK for driving sensors.
57	GPIO1<1>	PU	I/O	Also serves as output port for low frequency clock output.
55	FLASH_RDY		I/O	(GPIO1<4>)
53	TRIG		I/O	(GPIO1<5>)
52	MENU		I/O	(GPIO1<7>)
88	SELECT	PU	I/O	(GPIO2<0>)
89	SEN	PU	I/O	(GPIO2<1>)
90	SCK	PU	I/O	(GPIO2<2>)
91	SDA	PU	I/O	(GPIO2<3>)
92	RX		I/O	8051 UART0 RX in (GPIO2<4>)
93	TX		I/O	8051 UART0 TX out (GPIO2<5>)
96	GPIO2<7>		I/O	
67	GPIO3<6>		I/O	High speed UART2 RX
68	GPIO3<7>		I/O	High speed UART2 TX
127	GPIO4<0>	PU	I/O	8051 UART0 RX out (sync mode data out),
126	GPIO4<1>	PU	I/O	Timer1 clock input
65	GPIO6<3>	PU	I/O	
66	GPIO6<4>		I/O	
94	GPIO6<5>		I/O	
95	GPIO6<6>		I/O	
	Capture Interface			
71	CCLK		I	
73	CVREF		I/O	Also serves as the output port for generated VSYNC.
74	CHREF		I/O	Also serves as the output port for generated HSYNC.
75	CD<2>		I	
76	CD<3>		I	
77	CD<4>		I	
78	CD<5>		I	
80	CD<6>		I	
81	CD<7>		I	
82	CD<8>		I	
83	CD<9>		I	
	Misc.			
61	RST#		I	Hardware reset.

31	USB VDD		Power	3.3V
30	DMINUS		I/O	
29	DPLUS		I/O	
84	XIN		Osc	PLL OSC
85	XOUT		Osc	PLL OSC
51	Bat_low		Ana I	
	Power Pads			
14	VSS_IO		Power	Ground
28	VSS_IO		Power	
40	VSS_IO		Power	
64	VSS_IO		Power	
69	VSS_IO		Power	
87	VSS_IO		Power	
101	VSS_IO		Power	
113	VSS_IO		Power	
125	VSS_IO		Power	
17	VSS_CORE		Power	Ground
59	VSS_CORE		Power	
7	VDD_IO		Power	3.3V
21	VDD_IO		Power	
35	VDD_IO		Power	
54	VDD_IO		Power	
62	VDD_IO		Power	
79	VDD_IO		Power	
107	VDD_IO		Power	
121	VDD_IO		Power	
11	VDD_CORE		Power	1.8V
25	VDD_CORE		Power	
56	VDD_CORE		Power	
70	VDD_CORE		Power	
86	VDD_CORE		Power	
97	VDD_CORE		Power	
118	VDD_CORE		Power	
	Memory Interface			
128	MDQML		O	(MBE0)
6	MDQMH		O	RA13 for NOR flash. (MBE1)
				Power-on strapping on MD<15:0>
100	MD<0>	PU	I/O	PS<0> - Test Mode 0
102	MD<1>	PU	I/O	PS<1> - Test Mode 1
103	MD<2>	PU	I/O	PS<2> - Test Mode 2
104	MD<3>	PU	I/O	PS<3> - Clock Source
105	MD<4>	PU	I/O	PS<4> - External ROM
106	MD<5>	PU	I/O	PS<5> - CPU Boot

108	MD<6>	PU	I/O	PS<6> - USB Clock Div. 0
109	MD<7>	PU	I/O	PS<7> - USB Clock Div. 1
18	MD<8>	PU	I/O	PS<8> - USB PID 0
19	MD<9>	PU	I/O	PS<9> - USB PID 1
20	MD<10>	PU	I/O	PS<10> - USB PID 2
22	MD<11>	PU	I/O	PS<11> - USB PID 3
23	MD<12>	PU	I/O	PS<12> - USB PID 4
24	MD<13>	PU	I/O	PS<13> - USB PID 5
26	MD<14>	PU	I/O	PS<14> - USB Self Power
27	MD<15>	PU	I/O	PS<15> - USB High Power
120	MWE_B		O	
122	MCAS_B		O	
119	MRAS_B		O	
15	MBA<0>		O	
16	MBA<1>		O	
110	MA<0>		O	
111	MA<1>		O	
112	MA<2>		O	
114	MA<3>		O	
115	MA<4>		O	
116	MA<5>		O	
117	MA<6>		O	
8	MA<7>		O	
9	MA<8>		O	
10	MA<9>		O	
12	MA<10>		O	
13	MA<11>		O	
123	MCLK		O	
124	MCKE	PD	O	
98	CFCS2_B	PU	O	Also serves as SMCCS2_B and SDCMD.
2	SMCCS_B	PU	O	
1	ROMCS_B	PD	O	
99	CFCS1_B	PU	O	Also serves as SDCLK.
3	SDDATA<0>	PU	I/O	SD/MMC data, PS<16>
4	SDDATA<2>	PU	O	Also serves as WEb for CFC/SMC/NOR
5	SDDATA<3>	PU	O	Also serves as OEb/REb for CFC/SMC/NOR
	Display Interface			
49	LCD_HSYNC		O	
39	LCD_VSYNC		O	
50	LCD_CLK		O	
48	LCD_DATA_Eb		O	
38	LCD_DATA<2>		O	
37	LCD_DATA<3>		O	
36	LCD_DATA<4>		O	
34	LCD_DATA<5>		O	

33	LCD_DATA<6>		O	
32	LCD_DATA<7>		O	
	TV DAC			
47	TVDVSS		Power	
41	TVVDDIO		Power	3.3V
40	TVVSSIO		Power	
45	VCOMM		Ana O	
46	VREF		Ana I	
44	VRSET		Ana I	
43	VOUT		Ana O	Composite video output.

5. DC Characteristic:

5.1 Absolute Maximum Rating

Rating	Symbol	Value	Unit
DC supply voltage (IO)	VDDio	-0.3 to +4.0	V
DC supply voltage (core)	VDDcore	-0.3 to +2.0	V
Voltage, any pin to ground	V	-0.3 to VDD+0.3	V
DC current drain per pin (excluding VDD , VSS)	I	±10	mA
Operating temperature range	T_A	0 to +70	°C
Storage temperature range	Tstg	-65 to +150	°C

5.2 Electrical Characteristics (VDDio=3.3v, VDDcore=1.8V, T_A=0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
DC supply voltage (VDD_IO to GND)	VDDio	3.00	3.3	3.6	V
DC supply voltage (VDD to GND)	VDDcore	1.62	1.8	1.98	V
High level input voltage	V_{IH}	2.0		Vcc+0.3v	V
Low level input voltage	V_{IL}	-0.3		0.8	V
Input current (V_I=Vcc +0.3v or GND)	I_{IN}	-10	1	10	μA
Input capacitance	C_{IN}			10	pF
3-state output leakage current (V_O=Vcc +0.3v or GND)	I_{OZ}	-10	1	10	μA
Output capacitance	C_{OUT}			10	pF
High level output voltage (@Iout=-2ma)	V_{OH}	2.4		Vcc	V
Low level output voltage (@Iout=2ma)	V_{OL}	0		0.4	V
Crystal frequency (at XIN and XOUT pins)	F_{XLT}	5.88	12	24.012	MHz

5.3 USB VP/VM Pins Electrical Characteristics (VDDio=3.3v, VDDcore=1.8V, TA=0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Differential input sensitivity	V_{DI}	0.2			V
Differential common mode range	V_{CM}	0.8		2.5	V
Output signal crossover voltage	V_{CRS}	1.3		2.0	V
Single ended receiver threshold	V_{SE}	2.0		2.0	V
Static output low (@1.5kΩ pull up to 3.6v)	V_{OL}	0.0		0.3	V
Static output high (@15kΩ pull down to GND)	V_{OH}	2.8		3.6	V
Rise time	T_{FR}	4		20	ns
Fall time	T_{FF}	4		20	ns
Output resistance	Z_{DRV}	28		43	Ω
External D+, D- serial resistor	Rs		24		Ω