Product proposal

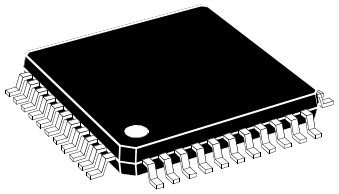
Triple 8-Bit Video DAC

CMOS

MC141685

The MC141685 contains three independent Digital to Analog Converters(DAC). The digital to analog conversion is accomplished by means of bank of binary controlled differential current sources.

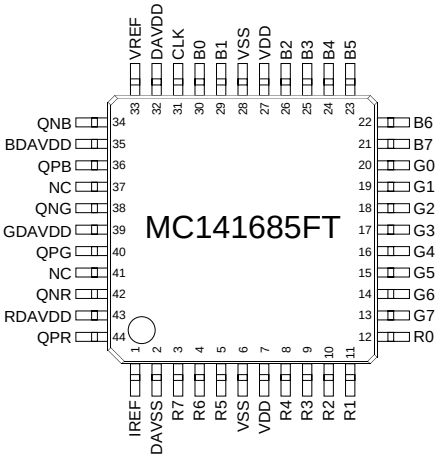
furthermore, differential outputs are provided. The MC141685 is especially suitable as a converter in TV-picture digital processing (e.g. picture-in picture), Video games, DVC, and DVD applications.



FT SUFFIX
CASE 824-F-01

Feature

Differential Outputs
Adjustable current output range.
TTL compatible input
Single 5V power supply



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (Ta= 25˚C unless otherwise specified)
Maximum ratings are those values beyond which damage to the device may occur.

Rating	Symbol	Value	Unit
Storage Temperature	Tstg	-65 to +150	˚C
Operating Ambient Temperature	TA	-20 to 80	˚C
Maximum Current Per Input Pin	Iin	±20	mA
Maximum Current Per Output pin	Iout	±50	mA
Maximum Voltage All Pins	Vin, Vout	-0.5 to VDD+0.5	V
Power Dissipation	Pd	700	mW
DC Supply Voltage	VDD	-0.5 to +6	V

ELECTRICAL CHARACTERISTICS (Ta=-20 to 80˚C unless otherwise specified; VDD=5.0V)

Characteristics	Symbol	Min	Typ	Max	Unit	remarks
Power supply Voltage	VDD	4.5	5.0	5.5	V	
Digital supply Current	DIDD	-	10	20	mA	
DAVDD(bias) Supply Current	DAIDD	-	4	12	mA	
DAVDD(for DAC) Supply current for Each DA Pins	RDAIDD GDAIdd BDAIdd	-	-	40	mA	
Internal Current Gain	K	3.0	3.5	4.0		
VREF Voltage	Vref	1.15	1.25	1.35	V	

ELECTRICAL CHARACTERISTICS (Ta=-20 to 80˚C unless otherwise specified; VDD=5.0V)
DA Converters

Characteristics	Symbol	Min	Typ	Max	Unit	remarks
Maximum Output Voltage	Vout	2.1	3.0	-	V	*1
Full Scale Output current	Iout	-	16	40	mA	
Differential Non-Linearity	DNL	-	-	±0.5	LSB	*2
Integral Non-Linearity	INL	-	-	±1.0	LSB	*2
DAC to DAC Max output Current Matching	ΔIout	-	2	5	%	
transition Time	Ttr	-	5	10	nS	*3
Analog Output delay Time	Td	-	50	-	nS	*3

*1. Rl=75Ω.
*2. Rbias=250Ω, Rl=75Ω.
*3. Rl=75Ω, Cl=15pF.

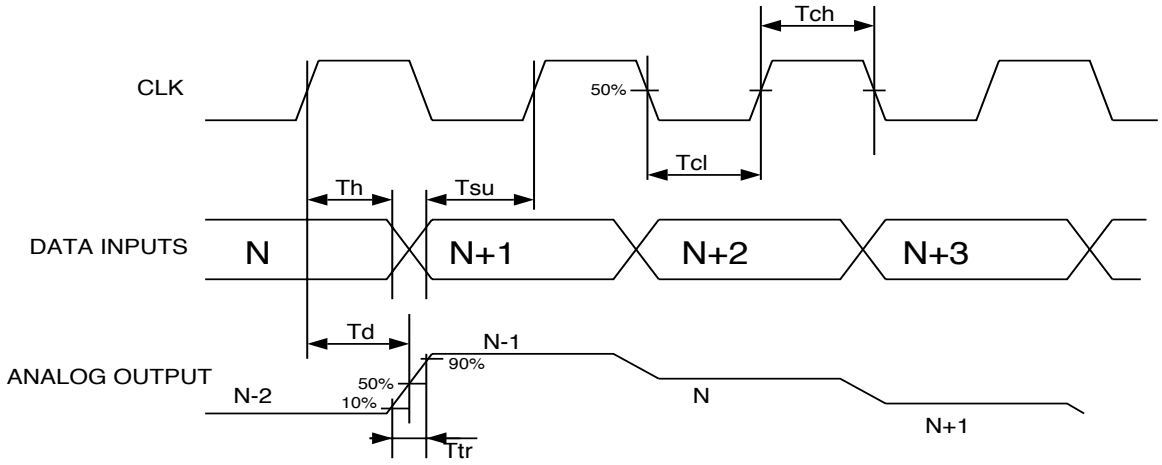
ELECTRICAL CHARACTERISTICS (Ta=-20 to 80˚C unless otherwise specified; VDD=5.0V)
Data Inputs

Characteristics	Symbol	Min	Typ	Max	Unit	remarks
Input High Level	VIH	2.2	-	-	V	
Input Low Level	VIL	-	-	1.0	V	
Data Setup Time	Tsu	4	-	-	nS	
Data Hold Time	Th	8	-	-	nS	

ELECTRICAL CHARACTERISTICS (Ta=-20 to 80˚C unless otherwise specified; VDD=5.0V)
Clock Input

Characteristics	Symbol	Min	Typ	Max	Unit	remarks
Clock Input Level	Vclk	500	-	-	mV	*4
Clock Input High Level	Vihc	3.5	-	-	V	
Clock Input Low Level	Vilc	-	-	1.5	V	
Clock Low Duration	Tcl	10	-	-	nS	
Clock High Duration	Tch	10	-	-	nS	

*4. When clock input as 0.1μ capacitor coupled input and waveform as sine wave.



Pin Assignments

PIN#	Name	I/O	Function
Pin1	IREF	-	Full scale current adjust control. Normally 3.3x of load is connected between this pin and DAVSS
Pin2	DAVSS	-	VSS of current reference circuit
Pin3	R7	I	b7 digital input for RDAC output QPR and QNR
Pin4	R6	I	b6 digital input for RDAC output QPR and QNR
Pin5	R5	I	b5 digital input for RDAC output QPR and QNR
Pin6	VSS	-	Digital VSS
Pin7	VDD	-	Digital Vdd
Pin8	R4	I	b4 digital input for RDAC output QPR and QNR
Pin9	R3	I	b3 digital input for RDAC output QPR and QNR
Pin10	R2	I	b2 digital input for RDAC output QPR and QNR
Pin11	R1	I	b1 digital input for RDAC output QPR and QNR
Pin12	R0	I	b0 digital input for RDAC output QPR and QNR
Pin13	G7	I	b7 digital input for GDAC output QPG and QNG
Pin14	G6	I	b6 digital input for GDAC output QPG and QNG
Pin15	G5	I	b5 digital input for GDAC output QPG and QNG
Pin16	G4	I	b4 digital input for GDAC output QPG and QNG
Pin17	G3	I	b3 digital input for GDAC output QPG and QNG
Pin18	G2	I	b2 digital input for GDAC output QPG and QNG
Pin19	G1	I	b1 digital input for GDAC output QPG and QNG
Pin20	G0	I	b0 digital input for GDAC output QPG and QNG
Pin21	B7	I	b7 digital input for BDAC output QPB and QNB
Pin22	B6	I	b6 digital input for BDAC output QPB and QNB
Pin23	B5	I	b5 digital input for BDAC output QPB and QNB
Pin24	B4	I	b4 digital input for BDAC output QPB and QNB
Pin25	B3	I	b3 digital input for BDAC output QPB and QNB
Pin26	B2	I	b2 digital input for BDAC output QPB and QNB
Pin27	VDD	-	Digital VDD
Pin28	VSS	-	Digital VSS
Pin29	B1	I	b1 digital input for BDAC output QPB and QNB
Pin30	B0	I	b0 digital input for BDAC output QPB and QNB
Pin31	CLK	I	Clock input. Rising edge clocks in new data to start conversion The clock buffer contain self-bias circuit, The clock input possible to operate using capacitor coupling clock input. typically, 0.1μF capacitor attach.
Pin32	DAVDD	-	VDD of current reference circuit
Pin33	VREF	I/O	This pin is an output voltage reference that is divided voltage between DAVDD and DAVSS by resister network. Typically, the pin outputs 1.25V when DAVDD=5V or it Can be over-driven using external voltage source of 1.2V
Pin34	QNB	O	complementary Current output pin for BDAC.
Pin35	BDAVDD	-	Power supply for BDAC
Pin36	QPB	O	Current output pin for BDAC.
Pin37	NC	-	Non-connection pin
Pin38	QNG	O	complementary Current output pin for GDAC.
Pin39	GDAVDD	-	Power supply for GDAC
Pin40	QPG	O	Current output pin for GDAC.
Pin41	NC	-	Non-connection pin
Pin42	QNR	O	complementary Current output pin for RDAC.
Pin43	RDAVDD	-	Power supply for RDAC
Pin44	QPR	O	Current output pin for RDAC.