SONY

CXD2545Q

CD Digital Signal Processor with Built-in Digital Servo

Description

The CXD2545Q is a digital signal processor IC with a built-in digital servo for CD players. This IC is broadly divided into a digital signal processor block and a digital servo block, and these blocks possess the following functions.

Digital Signal Processor Block

- Wide frame jitter margin (±28 frames) due to a built-in 32K RAM
- The bit clock, which strobes the EFM signal, is generated by the digital PLL.
- Enhanced EFM frame sync signal protection
- Refined super strategy-based powerful error correction
  C1: double correction, C2: quadruple correction
- Quadruple-speed, double-speed and variable pitch playback
- Noise reduction during track jumps
- Auto zero-cross mute
- Subcode demodulation and Sub Q data error detection
- Digital spindle servo (with oversampling filter)
- Asymmetry compensation circuit
- Error correction monitor signal, etc. output from a new CPU interface
- Servo auto sequencer
- Fine search performs track jumps with high accuracy
- Digital level meter, peak meter
- Bilingual compatible

Digital Servo Block

- Microcomputer software-based flexible servo control
- Servo error signal, offset cancel function
- Servo loop, auto gain control function
- E:F balance, focus bias adjustment function

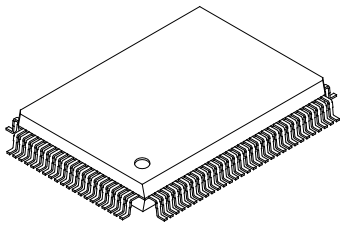
Features

- All digital signals produced during playback processed with a single chip
- Allows highly integrated chip mounting by incorporating the RAM and digital servo on-chip

Absolute Maximum Ratings

• Supply voltage	V_{DD}	–0.3 to 7.0	V
• Input voltage	V_I	–0.3 to +7.0	V
		(V_{SS} –0.3V to V_{DD} +0.3V)	
• Output voltage	V_O	–0.3 to +7.0	V
• Storage temperature	Tstg	–40 to +125	°C
• Supply voltage difference	V_{SS} – AV_{SS}	–0.3 to +0.3	V
	V_{DD} – AV_{DD}	–0.3 to +0.3	V

100 pin QFP (Plastic)



Recommended Operating Conditions

• Supply voltage	V_{DD}*	4.50 to 5.50	V
• Operating temperature	Topr	–20 to +75	°C

* The V_{DD} (min.) for the CXD2545Q varies according to the playback speed and built-in VCO selection. The V_{DD} (min.) is 4.50V when high-speed VCO and quadruple-speed playback are selected (variable pitch off). The V_{DD} (min.) for the CXD2545Q under various conditions are as shown in the following table.

Playback speed	V_{DD} (min.) [V]	
	VCO high speed	VCO normal speed
× 4	4.50	—
× 2*1	4.00	—
× 2	3.40	4.00
× 1	3.40	3.40
× 1*2	3.40	3.40

Dashes indicate that there is no assurance of the processor operating. All values are for variable pitch off.

*1 When the internal operation of the LSI is set to normal-speed playback and the operating clock of the signal processor is doubled, double-speed playback results.

*2 When the internal operation of the LSI is set to double-speed mode and the crystal oscillating frequency is halved in low power consumption mode, normal-speed playback results.

I/O Capacitance

• Input capacitance	C_I	12 (max.)	pF
• Output capacitance	C_O	12 (max.)	pF

When at high impedance

Note) Measurement conditions $V_{DD} = V_I = 0V$
$f_M = 1MHz$

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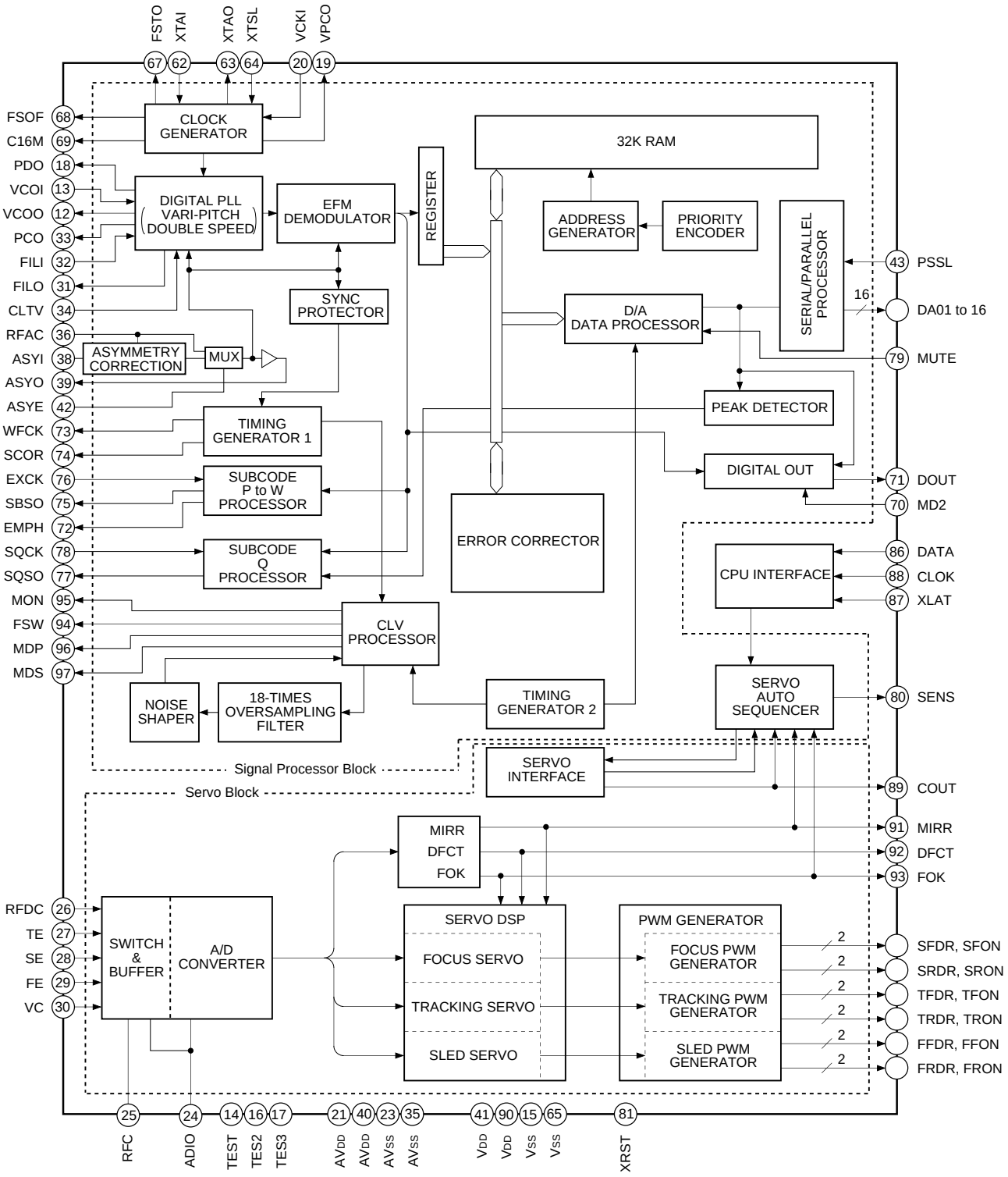
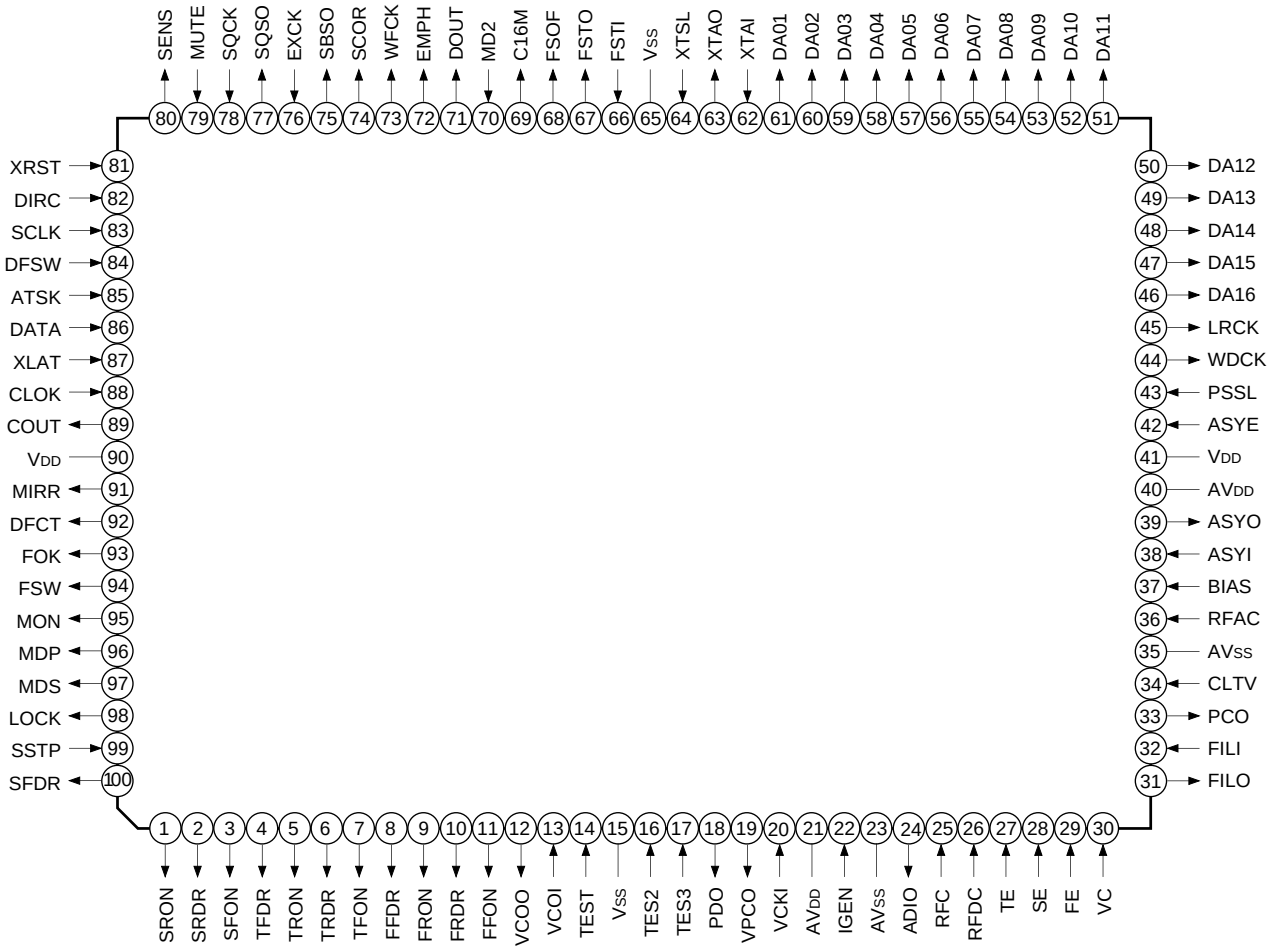
E95134A6X-PS

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	SRON	O	Sled drive output.
2	SRDR	O	Sled drive output.
3	SFON	O	Sled drive output.
4	TFDR	O	Tracking drive output.
5	TRON	O	Tracking drive output.
6	TRDR	O	Tracking drive output.
7	TFON	O	Tracking drive output.
8	FFDR	O	Focus drive output.
9	FRON	O	Focus drive output.
10	FRDR	O	Focus drive output.
11	FFON	O	Focus drive output.
12	VCOO	O	Analog EFM PLL oscillation circuit output.
13	VCOI	I	Analog EFM PLL oscillation circuit input. f_{LOCK} = 8.6436MHz.
14	TEST	I	Test pin. Normally GND.
15	V_{SS}	—	Digital GND.

Pin No.	Symbol	I/O	Description
16	TES2	I	Test pin. Normally GND.
17	TES3	I	Test pin. Normally GND.
18	PDO	O	Analog EFM PLL charge pump output.
19	VPCO	O	Variable pitch PLL charge pump output.
20	VCKI	I	Variable pitch clock input from the external VCO. fcenter = 16.9344MHz.
21	AV_{DD}	—	Analog power supply.
22	IGEN	I	Reference resistance connection for digital servo operational amplifier current source.
23	AV_{SS}	—	Analog GND.
24	ADIO	O	A/D converter input monitor.
25	RFC	I	RFDC input low-pass filter capacitor connection.
26	RFDC	I	RF signal input. Input range: 2.15 to 5.0V (when V_{DD} = AV_{DD} = 5.0V).
27	TE	I	Tracking error signal input. Input range: 2.5 ±1.0V (when V_{DD} = AV_{DD} = 5.0V).
28	SE	I	Sled error signal input. Input range: 2.5 ±1.0V (when V_{DD} = AV_{DD} = 5.0V).
29	FE	I	Focus error signal input. Input range: 2.5 ±1.0V (when V_{DD} = AV_{DD} = 5.0V).
30	VC	I	Center voltage input.
31	FILO	O	Master PLL filter output.
32	FILI	I	Master PLL filter input.
33	PCO	O	Master PLL charge pump output.
34	CLTV	I	Master PLL VCO control voltage input.
35	AV_{SS}	—	Analog GND.
36	RFAC	I	EFM signal input.
37	BIAS	I	Constant current input of asymmetry circuit.
38	ASYI	I	Comparator voltage input of asymmetry circuit.
39	ASYO	O	EFM full-swing output (low = V_{SS}, high = V_{DD}).
40	AV_{DD}	—	Analog power supply.
41	V_{DD}	—	Digital power supply.
42	ASYE	I	Asymmetry circuit on/off (low = off, high = on).
43	PSSL	I	Audio data output mode switching input. Low: serial output; high: parallel output.
44	WDCK	O	D/A interface and word clock for 48-bit slot. f = 2Fs.
45	LRCK	O	D/A interface and LR clock for 48-bit slot. f = Fs.
46	DA16	O	DA16 output when PSSL = 1. 48-bit slot serial data when PSSL = 0.
47	DA15	O	DA15 output when PSSL = 1. 48-bit slot bit clock when PSSL = 0.
48	DA14	O	DA14 output when PSSL = 1. 64-bit slot serial data when PSSL = 0.
49	DA13	O	DA13 output when PSSL = 1. 64-bit slot bit clock when PSSL = 0.
50	DA12	O	DA12 output when PSSL = 1. 64-bit slot LR clock when PSSL = 0.
51	DA11	O	DA11 output when PSSL = 1. GTOP output when PSSL = 0.
52	DA10	O	DA10 output when PSSL = 1. XUGF output when PSSL = 0.

Pin No.	Symbol	I/O	Description
53	DA09	O	DA09 output when PSSL = 1. XPLCK output when PSSL = 0.
54	DA08	O	DA08 output when PSSL = 1. GFS output when PSSL = 0.
55	DA07	O	DA07 output when PSSL = 1. RFCK output when PSSL = 0.
56	DA06	O	DA06 output when PSSL = 1. C2PO output when PSSL = 0.
57	DA05	O	DA05 output when PSSL = 1. XRAOF output when PSSL = 0.
58	DA04	O	DA04 output when PSSL = 1. MNT3 output when PSSL = 0.
59	DA03	O	DA03 output when PSSL = 1. MNT2 output when PSSL = 0.
60	DA02	O	DA02 output when PSSL = 1. MNT1 output when PSSL = 0.
61	DA01	O	DA01 output when PSSL = 1. MNT0 output when PSSL = 0.
62	XTAI	I	Crystal oscillation circuit input. Input 16.9344MHz or 33.8688MHz.
63	XTAO	O	Crystal oscillation circuit output.
64	XTSL	I	Crystal selector input. Low when the crystal is 16.9344MHz; high when the crystal is 33.8688MHz (during normal-speed playback).
65	V_{SS}	—	Digital GND.
66	FSTI	I	Digital servo block reference clock input.
67	FSTO	O	2/3 frequency divider output for Pins 62 and 63. This pin does not change with variable pitch.
68	FSOF	O	1/4 frequency divider output for Pins 62 and 63. This pin does not change with variable pitch.
69	C16M	O	16.9344MHz output. This pin changes simultaneously with the variable pitch (during normal-speed playback).
70	MD2	I	Digital Out on/off control (low = off, high = on).
71	DOUT	O	Digital Out output.
72	EMPH	O	Playback disc emphasis mode output. (Outputs a high signal when the playback disc has emphasis, and a low signal when there is no emphasis.)
73	WFCK	O	WFCK output.
74	SCOR	O	Subcode sync output. (Outputs a high signal when either subcode sync S0 or S1 is detected.)
75	SBSO	O	Sub P to W serial output.
76	EXCK	I	SBSO readout clock input.
77	SQSO	O	Sub Q 80-bit output. PCM peak and level data 16-bit output.
78	SQCK	I	SQSO readout clock input.
79	MUTE	I	Mute switching pin (high: mute).
80	SENS	O	SENS output to CPU.
81	XRST	I	System reset (reset when low).
82	DIRC	I	Used for 1 track jumps. (Input V_{DD} level when not used.)
83	SCLK	I	SENS serial data readout clock.
84	DFSW	I	DFCT switching pin (high: DFCT countermeasure circuit off).
85	ATSK	I	Anti-shock pin.

Pin No.	Symbol	I/O	Description
86	DATA	I	Serial data input from CPU.
87	XLAT	I	Latch input from CPU.
88	CLOK	I	Serial data transfer clock input from CPU.
89	COUT	O	Track count signal input.
90	V_{DD}	—	Digital power supply.
91	MIRR	O	Mirror signal output.
92	DFCT	O	Defect signal output.
93	FOK	O	Focus OK output.
94	FSW	O	Spindle motor output filter switching output.
95	MON	O	Spindle motor on/off control output.
96	MDP	O	Spindle motor servo control.
97	MDS	O	Spindle motor servo control.
98	LOCK	O	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low.
99	SSTP	I	Disc innermost track detective signal pin.
100	SFDR	O	Sled drive output.

Notes)
- The 64-bit slot is an LSB first, two's complement output. The 48-bit slot is an MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window released.)
- XUGF is the negative pulse for the frame sync obtained from the EFM signal. It is the signal before sync protection.
- XPLCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- The GFS signal goes high when the frame sync and the insertion protection timing match.
- RFCK is derived from the crystal accuracy, and has a cycle of 136µs.
- C2PO represents the data error status.
- XRAOF is generated when the 32K RAM exceeds the ±28 F jitter margin.

Electrical Characteristics

1. DC Characteristics

(V_{DD} = AV_{DD} = 5.0V ±10%, Vss = AVss = 0V, Topr = –20 to +75°C)

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		0.7V_{DD}			V	*1
	Low level input voltage	V_{IL} (1)				0.3V_{DD}	V	
Input voltage (2)	High level input voltage	V_{IH} (2)	Schmitt input	0.8V_{DD}			V	*2
	Low level input voltage	V_{IL} (2)				0.2V_{DD}	V	
Input voltage (3)	Input voltage	V_{IN} (3)	Analog input	Vss		V_{DD}	V	*3, 11
Output voltage (1)	High level output voltage	V_{OH}(1)	I_{OH} = –4mA	V_{DD} – 0.8		V_{DD}	V	*4
	Low level output voltage	V_{OL}(1)	I_{OL} = 4mA	0		0.4	V	
Output voltage (2)	High level output voltage	V_{OH}(2)	I_{OH} = –2mA	V_{DD} – 0.8		V_{DD}	V	*5
	Low level output voltage	V_{OL} (2)	I_{OL} = 4mA	0		0.4	V	
Output voltage (3)	Low level output voltage	V_{OL} (3)	I_{OL} = 4mA	0		0.4	V	*6
Output voltage (4)	High level output voltage	V_{OH}(4)	I_{OH} = –0.28mA	V_{DD} – 0.5		V_{DD}	V	*7
	Low level output voltage	V_{OL} (4)	I_{OL} = 0.36mA	0		0.4	V	
Input leak current (1)		I_{LI} (1)	V_I = 0 to 5.5V	–10		10	µA	*1, 2, 3
Input leak current (2)		I_{LI} (2)	V_I = 1.5 to 3.5V	–20		20	µA	*8
Input leak current (3)		I_{LI} (3)	V_I = 0 to 5.0V	–40		600	µA	*9
Tri-state pin output leak current		I_{LO}	V_O = 0 to 5.5V	–5		5	µA	*10

Applicable pins

*1 XTSL, DATA, XLAT, MD2, PSSL, TEST, TES2, TES3, DFSW, DIRC, SSTP, ATSK

*2 CLOK, XRST, EXCK, SQCK, MUTE, VCKI, ASYE, FSTI, SCLK

*3 CLTV, FILI, RFAC, ASYI, RFDC, TE, SE, FE, VC

*4 MDP, PDO, PCO, VPCO

*5 ASYO, DOUT, FSTO, FSOF, C16M, SBSO, SQSO, SCOR, EMPH, MON, LOCK, WDCK, SENS, MDS, DA01 to DA16, LRCK, WFCK, FOK, COUT, MIRR, DFCT, FFON, FRDR, FRON, FFDR, TFON, TRDR, TRON, TFDR, SFON, SRDR, SRON, SFDR

*6 FSW

*7 FILO

*8 TE, SE, FE, VC

*9 RFDC

*10 SENS, MDS, MDP, FSW, PDO, PCO, VPCO

*11 RFC

2. AC Characteristics

(1) XTAI pin, VCOI pin

(a) When using self-excited oscillation

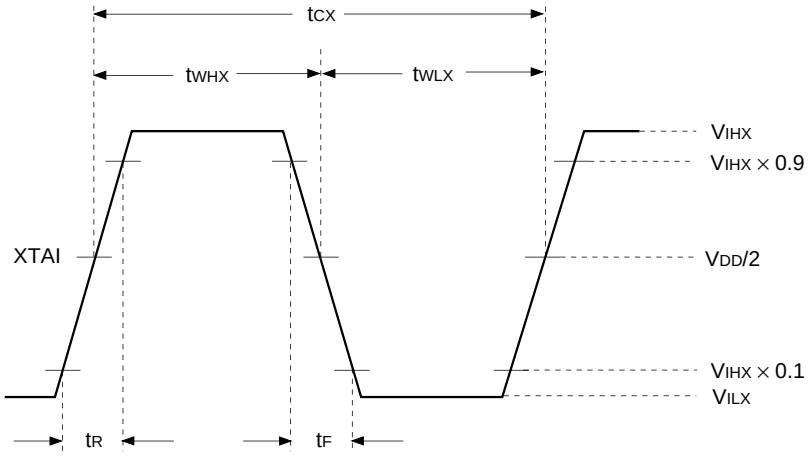
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ±10%)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	7		34	MHz

(b) When inputting pulses to XTAI and VCOI

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ±10%)

Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}	13		500	ns
Low level pulse width	t_{WLX}	13		500	ns
Pulse cycle	t_{CX}	26		1000	ns
Input high level	V_{IHX}	V_{DD} – 1.0			V
Input low level	V_{ILX}			0.8	V
Rise time, fall time	t_R, t_F			10	ns



(c) When inputting sine waves to the XTAI and VCOI pins via a capacitor

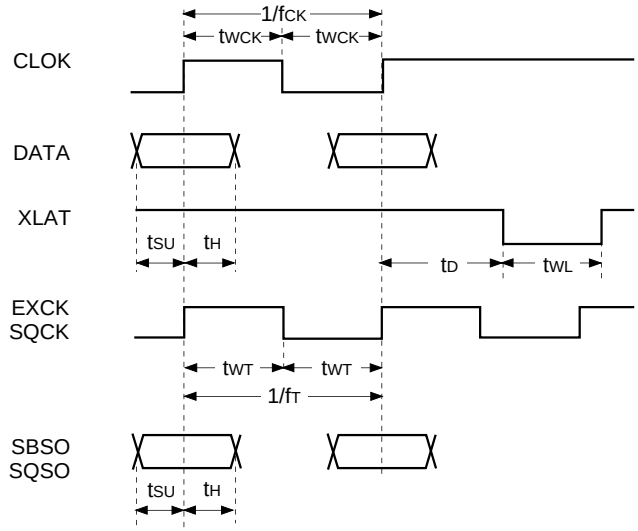
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ±10%)

Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_I	2.0		V_{DD} + 0.3	Vp-p

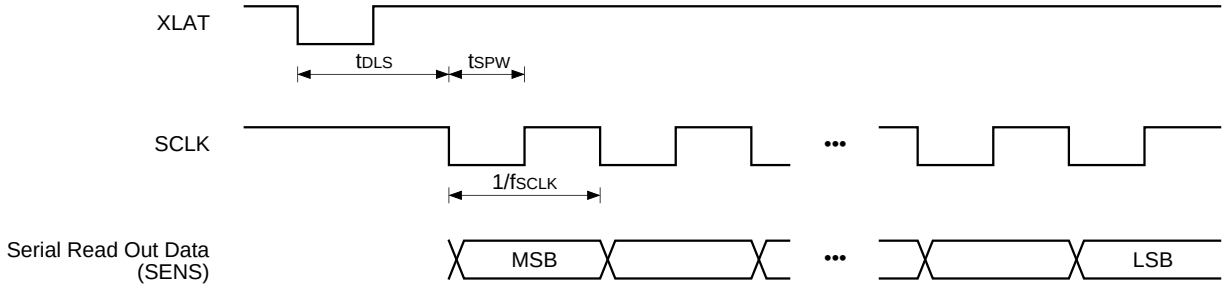
(2) CLOK, DATA, XLAT, SQCK and EXCK pins

(V_{DD} = AV_{DD} = 5.0V ±10%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			0.65	MHz
Clock pulse width	t_{WCK}	750			ns
Setup time	t_{SU}	300			ns
Hold time	t_H	300			ns
Delay time	t_D	300			ns
Latch pulse width	t_{WL}	750			ns
EXCK SQCK frequency	f_T			0.65	MHz
EXCK SQCK pulse width	t_{WT}	750			ns



(3) SCLK pin



Item	Symbol	Min.	Typ.	Max.	Unit
SCLK frequency	f_{SCLK}			1	MHz
SCLK pulse width	t_{SPW}	500			ns
Delay time	t_{DLS}	15			µs

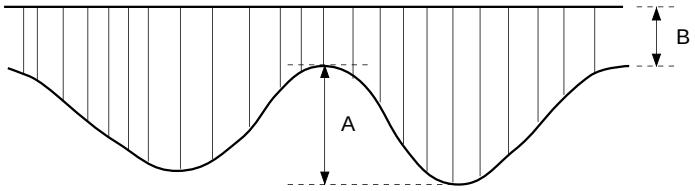
(4) COUT, MIRR and DFCT pins

Operating frequency (V_{DD} = AV_{DD} = 5.0V ±10%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
COUT maximum operating frequency	f_{COUT}	40			kHz	*1
MIRR maximum operating frequency	f_{MIRR}	40			kHz	*2
DFCT maximum operating frequency	f_{DFCTH}	5			kHz	*3

*1 When using a high-speed traverse TZC.

*2



When the RF signal continuously satisfies the following conditions during the above traverse.

- A = 0.6 to 1.3V
- $\frac{B}{A + B}$ = less than 25%

*3 During complete RF signal omission.
When settings related to DFCT signal generation are Typ.

Contents

Explanation of abbreviations

AVRG:	Average
AGCNTL:	Automatic gain control
FCS:	Focus
TRK:	Tracking
SLD:	Sled
DFCT:	Defect

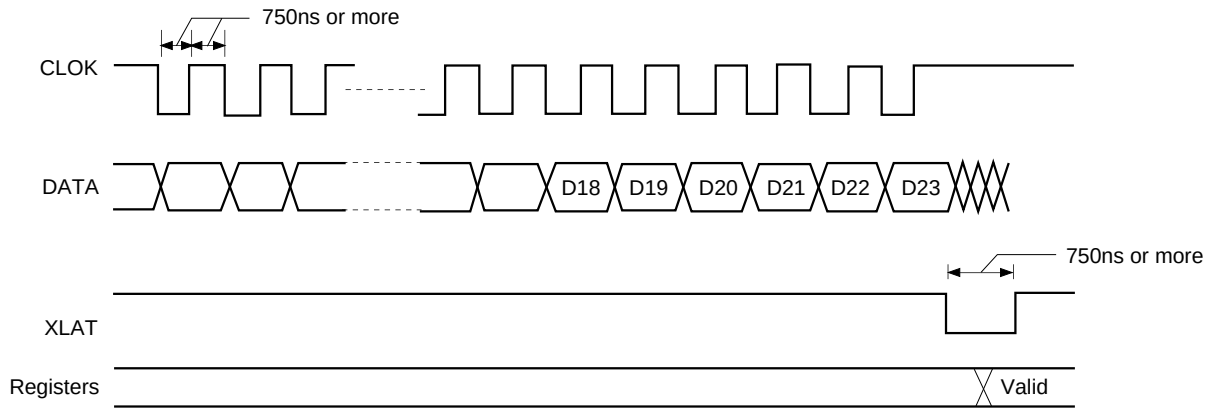
[1] CPU Interface

§1-1. CPU Interface Timing

• CPU interface

This interface uses DATA, CLOK and XLAT to set the modes.

The interface timing chart is shown below.



• The internal registers are initialized by a reset when XRST = 0.

§1-2. CPU Interface Command Table

Total bit length for each register

Register	Total bit length
0 to 2	8bit
3	8 to 24bit
4 to 6	16bit
7	20bit
8 to A	16bit
B	20bit
C to E	16bit

Command Table ($0X to 1X)

Register	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	FOCUS CONTROL	0 0 0 0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO ON (FOCUS GAIN NORMAL)
			1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO ON (FOCUS GAIN DOWN)
			0	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, 0V OUT
			0	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT
			0	—	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SEARCH VOLTAGE DOWN
			0	—	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SEACH VOLTAGE UP
1	TRACKING CONTROL	0 0 0 1	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANTI SHOCK ON
			0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANTI SHOCK OFF
			—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BRAKE ON
			—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BRAKE OFF
			—	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN NORMAL
			—	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP
			—	—	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 1
			—	—	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 2

—: Don’t care

Command Table ($2X to 3X)

Register	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
2	TRACKING MODE	0 0 1 0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO OFF
			0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO ON
			1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FORWARD TRACK JUMP
			1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REVERSE TRACK JUMP
			—	—	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED SERVO OFF
			—	—	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED SERVO ON
			—	—	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FORWARD SLED MOVE
			—	—	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REVERSE SLED MOVE

Register	Command	Address		Data 1		Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±1 + basic value) (Default)
			0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±2 + basic value)
			0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±3 + basic value)
			0	0	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±4 + basic value)

—: Don't care

Command Table ($340X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0000	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K00) SLED INPUT GAIN
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K01) SLED LOW BOOST FILTER A-H
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K02) SLED LOW BOOST FILTER A-L
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K03) SLED LOW BOOST FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K04) SLED LOW BOOST FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K05) SLED OUTPUT GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K06) FOCUS INPUT GAIN
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K07) SLED AUTO GAIN
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K08) FOCUS HIGH CUT FILTER A
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K09) FOCUS HIGH CUT FILTER B
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0A) FOCUS LOW BOOST FILTER A-H
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0B) FOCUS LOW BOOST FILTER A-L
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0C) FOCUS LOW BOOST FILTER B-H
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0D) FOCUS LOW BOOST FILTER B-L
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0E) FOCUS PHASE COMPENSATE FILTER A
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0F) FOCUS DEFECT HOLD GAIN

Command Table ($341X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0001	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K10) FOCUS PHASE COMPENSATE FILTER B
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K11) FOCUS OUTPUT GAIN
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K12) ANTI SHOCK INPUT GAIN
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K13) FOCUS AUTO GAIN
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K14) HPTZC / AUTO GAIN HIGH PASS FILTER A
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K15) HPTZC / AUTO GAIN HIGH PASS FILTER B
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K16) ANTI SHOCK HIGH PASS FILTER A
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K17) HPTZC / AUTO GAIN LOW PASS FILTER B
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K18) FIX
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K19) TRACKING INPUT GAIN
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1A) TRACKING HIGH CUT FILTER A
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1B) TRACKING HIGH CUT FILTER B
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1C) TRACKING LOW BOOST FILTER A-H
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1D) TRACKING LOW BOOST FILTER A-L
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1E) TRACKING LOW BOOST FILTER B-H
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1F) TRACKING LOW BOOST FILTER B-L

Command Table ($342X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0010	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K20) TRACKING PHASE COMPENSATE FILTER A
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K21) TRACKING PHASE COMPENSATE FILTER B
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K22) TRACKING OUTPUT GAIN
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K23) TRACKING AUTO GAIN
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K24) FOCUS GAIN DOWN HIGH CUT FILTER A
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K25) FOCUS GAIN DOWN HIGH CUT FILTER B
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K26) FOCUS GAIN DOWN LOW BOOST FILTER A-H
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K27) FOCUS GAIN DOWN LOW BOOST FILTER A-L
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K28) FOCUS GAIN DOWN LOW BOOST FILTER B-H
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K29) FOCUS GAIN DOWN LOW BOOST FILTER B-L
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2A) FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2B) FOCUS GAIN DOWN DEFECT HOLD GAIN
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2C) FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2D) FOCUS GAIN DOWN OUTPUT GAIN
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2E) NOT USED
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2F) NOT USED

Command Table ($343X)

Regiater	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0011	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K30) FIX
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K31) ANTI SHOCK LOW PASS FILTER B
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K32) NOT USED
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K33) ANTI SHOCK HIGH PASS FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K34) ANTI SHOCK HIGH PASS FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K35) ANTI SHOCK FILTER COMPARATE GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K36) TRACKING GAIN UP2 HIGH CUT FILTER A
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K37) TRACKING GAIN UP2 HIGH CUT FILTER B
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K38) TRACKING GAIN UP2 LOW BOOST FILTER A-H
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K39) TRACKING GAIN UP2 LOW BOOST FILTER A-L
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3A) TRACKING GAIN UP2 LOW BOOST FILTER B-H
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3B) TRACKING GAIN UP2 LOW BOOST FILTER B-L
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3C) TRACKING GAIN UP PHASE COMPENSATE FILTER A
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3D) TRACKING GAIN UP PHASE COMPENSATE FILTER B
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3E) TRACKING GAIN UP OUTPUT GAIN
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3F) NOT USED

Command Table ($344X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0100	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K40) TRACKING HOLD FILTER INPUT GAIN
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K41) TRACKING HOLD FILTER A-H
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K42) TRACKING HOLD FILTER A-L
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K43) TRACKING HOLD FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K44) TRACKING HOLD FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K45) TRACKING HOLD FILTER OUTPUT GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K46) NOT USED
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K47) NOT USED
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K48) FOCUS HOLD FILTER INPUT GAIN
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K49) FOCUS HOLD FILTER A-H
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4A) FOCUS HOLD FILTER A-L
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4B) FOCUS HOLD FILTER B-H
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4C) FOCUS HOLD FILTER B-L
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4D) FOCUS HOLD FILTER OUTPUT GAIN
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4E) NOT USED
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4F) NOT USED

Command Table ($34FX to 3FX)

Register	Command	Address 1					Address 2						Data 1		Data 2				Data 3				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	1	0	0	1	1	1	1	0	1	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	—	FOCUS BIAS DATA
		0 0 1 1	0	1	0	0	1	1	1	1	0	0	TV9	TV8	TV7	TV6	TV5	TV4	TV3	TV2	TV1	TV0	TRVSC DATA
		Address					Data 1				Data 2				Data 3				Data 4				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0 0 1 1	0	1	0	1	FT1	FT0	FS5	FS4	FS3	FS2	FS1	FS0	FTZ	FG6	FG5	FG4	FG3	FG2	FG1	FG0	FOCUS SEARCH SPEED/ VOLTAGE/AUTO GAIN
			0	1	1	0	0	DTZC	TJ5	TJ4	TJ3	TJ2	TJ1	TJ0	0	TG6	TG5	TG4	TG3	TG2	TG1	TG0	DTZC/TRACK JUMP VOLTAGE/AUTO GAIN
			0	1	1	1	FZSH	FZSL	SM5	SM4	SM3	SM2	SM1	SM0	AGS	AGJ	AGGF	AGGT	AGV1	AGV2	AGHS	AGHT	FZSL/SLED MOVE/ Voltage/AUTO GAIN
			1	0	0	0	VCLM	VCLC	FLM	FLC0	RFLM	RFLC	AGF	AGT	DFSW	LKSW	TBLM	TCLM	FLC1	TLC2	TLC1	TLC0	LEVEL/AUTO GAIN/ DFSW/ (Initialize)
			1	0	0	1	DAC	SD6	SD5	SD4	SD3	SD2	SD1	SD0	0	0	0	0	0	0	0	0	SERIAL DATA READ MODE/SELECT
			1	0	1	0	0	FBON	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FOCUS BIAS
			1	0	1	1	SFO2	SFO1	SDF2	SDF1	MAX2	MAX1	SFOX	BTF	D2V2	D2V1	D1V2	D1V1	0	0	0	0	Operation for MIRR/ DFCT/FOK
		Address					Data 1				Data 2				Data 3				Data 4				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0 0 1 1	1	1	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TZC for COUT SLCT HPTZC (Default)
			1	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TZC for COUT SLCT DTZC
		Address					Data 1				Data 2				Data 3				Data 4				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0 0 1 1	1	1	1	0	F1NM	F1DM	F3NM	F3DM	T1NM	T1UM	T3NM	T3UM	DFIS	TLCD	RFLP	0	0	0	0	0	Filter
			1	1	1	1	0	0	XT4D	XT2D	0	DRR2	DRR1	DRR0	0	ASFG	0	LPAS	SRO1	SRO0	0	0	Others

—: Don't care

Command Table ($4X to EX)

Register	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5			
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
4	Auto sequence	0 1 0 0	AS3	AS2	AS1	AS0	MT3	MT2	MT1	MT0	LSSL	0	0	0	—	—	—	—	—	—	—	—
5	Blind (A, E), Brake (B), Overflow (C, D)	0 1 0 1	TR3	TR2	TR1	TR0	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
6	Sled kick, brake (D), Kick (F)	0 1 1 0	SD3	SD2	SD1	SD0	KF3	KF2	KF1	KF0	0	0	0	0	—	—	—	—	—	—	—	—
7	Auto sequence (N) track jump count setting	0 1 1 1	32,768	16,384	8,192	4,096	2,048	1,024	512	256	128	64	32	16	8	4	2	1	—	—	—	—
8	MODE setting	1 0 0 0	CD-ROM	DOUT Mute	D. out Mute-F	WSEL	VCO SEL	ASHS	SOCT	0	0	0	0	0	—	—	—	—	—	—	—	—
9	Function specification	1 0 0 1	DCLV ON-OFF	DSPB ON-OFF	ASEQ ON-OFF	DPLL ON-OFF	BiliGL MAIN	BiliGL SUB	FLFC	0	0	0	0	0	—	—	—	—	—	—	—	—
A	Audio CTRL	1 0 1 0	Vari Up	Vari Down	Mute	ATT	PTC1	PTC2	0	0	0	0	0	0	—	—	—	—	—	—	—	—
B	Traverse monitor counter setting	1 0 1 1	32,768	16,384	8,192	4,096	2,048	1,024	512	256	128	64	32	16	8	4	2	1	—	—	—	—
C	Spindle servo coefficient setting	1 1 0 0	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	0	Gain DCLV0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
D	CLV CTRL	1 1 0 1	DCLV PWM MD	TB	TP	Gain CLVS	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
E	CLV MODE	1 1 1 0	CM3	CM2	CM1	CM0	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—

—: Don't care

§1-3. CPU Command Presets

Command Preset Table ($0X to 34X)

Register	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	FOCUS CONTROL	0 0 0 0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, 0V OUT
1	TRACKING CONTROL	0 0 0 1	0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 1
2	TRACKING MODE	0 0 1 0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO OFF SLED SERVO OFF
Register	Command	Address			Data 1		Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D0	D0	
3	SELECT	0 0 1 1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±1 + basic value) (Default)
		Address 1					Address 2				Address 3				Data 1				Data 2				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D0	D0	
		0 0 1 1	0	1	0	0	0	See the coefficient preset values table.															KRAM DATA ($3400XX to $344fXX)

—: Don't care

Command Preset Table ($34FX to 3FX)

Register	Command	Address 1					Address 2						Data 1		Data 2				Data 3				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	1	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	—	FOCUS BIAS DATA
		0 0 1 1	0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	TRVSC DATA
		Address					Data 1				Data 2				Data 3				Data 4				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0 0 1 1	0	1	0	1	0	1	0	1	1	0	0	0	0	0	1	0	1	1	0	1	FOCUS SEARCH SPEED/ VOLTAGE/AUTO GAIN
			0	1	1	0	0	0	0	0	1	1	1	0	0	0	1	0	1	1	1	0	DTZC/TRACK JUMP VOLTAGE/AUTO GAIN
			0	1	1	1	0	1	0	1	0	0	0	0	1	0	1	1	1	0	1	0	FZSL/SLED MOVE/ Voltage/AUTO GAIN
			1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LEVEL/AUTO GAIN/ DFSW/ (Initialize)
			1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SERIAL DATA READ MODE/SELECT
			1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FOCUS BIAS
			1	0	1	1	1	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	Operation for MIRR/ DFCT/FOK
		Address				Data 1					Data 2				Data 3				Data 4				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0 0 1 1	1	1	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TZC for COUT SLCT HPTZC
		Address					Data 1				Data 2				Data 3				Data 4				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0 0 0 1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Filter
			1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Others

—: Don't care

Command Preset Table ($4X to EX)

Register	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5			
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
4	Auto sequence	0 1 0 0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
5	Blind (A, E), Brake (B), Overflow (C, D)	0 1 0 1	0	1	0	1	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
6	Sled kick, brake (D), Kick (F)	0 1 1 0	0	1	1	1	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
7	Auto sequence (N) track jump count setting	0 1 1 1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	—	—	—	—
8	MODE setting	1 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
9	Function specification	1 0 0 1	1	0	0	1	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
A	Audio CTRL	1 0 1 0	0	0	1	1	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
B	Traverse monitor counter setting	1 0 1 1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	—	—	—	—
C	Spindle servo coefficient setting	1 1 0 0	0	1	1	0	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
D	CLV CTRL	1 1 0 1	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
E	CLV MODE	1 1 1 0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—

—: Don't care

<Coefficient ROM Preset Values Table (1)>

ADDRESS	DATA	CONTENTS
K00	E0	SLED INPUT GAIN
K01	81	SLED LOW BOOST FILTER A-H
K02	23	SLED LOW BOOST FILTER A-L
K03	7F	SLED LOW BOOST FILTER B-H
K04	6A	SLED LOW BOOST FILTER B-L
K05	10	SLED OUTPUT GAIN
K06	14	FOCUS INPUT GAIN
K07	30	SLED AUTO GAIN
K08	7F	FOCUS HIGH CUT FILTER A
K09	46	FOCUS HIGH CUT FILTER B
K0A	81	FOCUS LOW BOOST FILTER A-H
K0B	1C	FOCUS LOW BOOST FILTER A-L
K0C	7F	FOCUS LOW BOOST FILTER B-H
K0D	58	FOCUS LOW BOOST FILTER B-L
K0E	82	FOCUS PHASE COMPENSATE FILTER A
K0F	7F	FOCUS DEFECT HOLD GAIN
K10	4E	FOCUS PHASE COMPENSATE FILTER B
K11	32	FOCUS OUTPUT GAIN
K12	20	ANTI SHOCK INPUT GAIN
K13	30	FOCUS AUTO GAIN
K14	80	HPTZC / Auto Gain HIGH PASS FILTER A
K15	77	HPTZC / Auto Gain HIGH PASS FILTER B
K16	80	ANTI SHOCK HIGH PASS FILTER A
K17	77	HPTZC / Auto Gain LOW PASS FILTER B
K18	00	Fix*
K19	F1	TRACKING INPUT GAIN
K1A	7F	TRACKING HIGH CUT FILTER A
K1B	3B	TRACKING HIGH CUT FILTER B
K1C	81	TRACKING LOW BOOST FILTER A-H
K1D	44	TRACKING LOW BOOST FILTER A-L
K1E	7F	TRACKING LOW BOOST FILTER B-H
K1F	5E	TRACKING LOW BOOST FILTER B-L
K20	82	TRACKING PHASE COMPENSATE FILTER A
K21	44	TRACKING PHASE COMPENSATE FILTER B
K22	18	TRACKING OUTPUT GAIN
K23	30	TRACKING AUTO GAIN
K24	7F	FOCUS GAIN DOWN HIGH CUT FILTER A
K25	46	FOCUS GAIN DOWN HIGH CUT FILTER B
K26	81	FOCUS GAIN DOWN LOW BOOST FILTER A-H
K27	3A	FOCUS GAIN DOWN LOW BOOST FILTER A-L
K28	7F	FOCUS GAIN DOWN LOW BOOST FILTER B-H
K29	66	FOCUS GAIN DOWN LOW BOOST FILTER B-L
K2A	82	FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
K2B	44	FOCUS GAIN DOWN DEFECT HOLD GAIN
K2C	4E	FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
K2D	1B	FOCUS GAIN DOWN OUTPUT GAIN
K2E	00	NOT USED
K2F	00	NOT USED

<Coefficient ROM Preset Values Table (2)>

ADDRESS	DATA	CONTENTS
K30	80	Fix*
K31	66	ANTI SHOCK LOW PASS FILTER B
K32	00	NOT USED
K33	7F	ANTI SHOCK HIGH PASS FILTER B-H
K34	6E	ANTI SHOCK HIGH PASS FILTER B-L
K35	20	ANTI SHOCK FILTER COMPARATE GAIN
K36	7F	TRACKING GAIN UP2 HIGH CUT FILTER A
K37	3B	TRACKING GAIN UP2 HIGH CUT FILTER B
K38	80	TRACKING GAIN UP2 LOW BOOST FILTER A-H
K39	44	TRACKING GAIN UP2 LOW BOOST FILTER A-L
K3A	7F	TRACKING GAIN UP2 LOW BOOST FILTER B-H
K3B	77	TRACKING GAIN UP2 LOW BOOST FILTER B-L
K3C	86	TRACKING GAIN UP PHASE COMPENSATE FILTER A
K3D	0D	TRACKING GAIN UP PHASE COMPENSATE FILTER B
K3E	57	TRACKING GAIN UP OUTPUT GAIN
K3F	00	NOT USED
K40	04	TRACKING HOLD FILTER INPUT GAIN
K41	7F	TRACKING HOLD FILTER A-H
K42	7F	TRACKING HOLD FILTER A-L
K43	79	TRACKING HOLD FILTER B-H
K44	17	TRACKING HOLD FILTER B-L
K45	6D	TRACKING HOLD FILTER OUTPUT GAIN
K46	00	NOT USED
K47	00	NOT USED
K48	02	FOCUS HOLD FILTER INPUT GAIN
K49	7F	FOCUS HOLD FILTER A-H
K4A	7F	FOCUS HOLD FILTER A-L
K4B	79	FOCUS HOLD FILTER B-H
K4C	17	FOCUS HOLD FILTER B-L
K4D	54	FOCUS HOLD FILTER OUTPUT GAIN
K4E	00	NOT USED
K4F	00	NOT USED

* Fix indicates that normal preset values should be used.

§1-4. Description of SENS Signals

SENS output

Microcomputer serial register (latching not required)	ASEQ = 0	ASEQ = 1	Output data length
$0X	Z	FZC	—
$1X	Z	AS	—
$2X	Z	TZC	—
$38	Z	AGOK*1	—
$38	Z	XAVEBSY*1	—
$30 to 37, $3A to 3F	Z	SSTP	—
$3904	Z	TE Avrg Reg.	9 bit
$3908	Z	FE Avrg Reg.	9 bit
$390C	Z	VC Avrg Reg.	9 bit
$391C	Z	TRVSC Reg.	9 bit
$391D	Z	FB Reg.	9 bit
$391F	Z	RFDC Avrg Reg.	8 bit
$4X	Z	XBUSY	—
$5X	Z	FOK	—
$6X	Z	0	—
$AX	GFS	GFS	—
$BX	COMP	COMP	—
$CX	COUT	COUT	—
$EX	$\overline{OV64}$	$\overline{OV64}$	—
$7X, 8X, 9X, DX, FX	Z	0	—

*1 $38 outputs AGOK during AGT and AGF command settings, and XAVEBSY during AVRG measurement. SSTP is output in all other cases.

Description of SENS Signals

SENS output	
Z	The SENS pin is high impedance.
XBUSY	Low while the auto sequencer is in operation, high when operation terminates.
FOK	Outputs the same signal as the FOK pin. High for "focus OK".
GFS	High when the regenerated frame sync is obtained with the correct timing.
COMP	Counts the number of tracks set with Reg B. High when Reg B is latched, low when the initial Reg B number is input by CNIN.
COUT	Counts the number of tracks set with Reg B. High when Reg B is latched, toggles each time the Reg B number is input by CNIN. While $44 and $45 are being executed, toggles with each CNIN 8-count instead of the Reg B number.
$\overline{\text{OV64}}$	Low when the EFM signal, after passing through the sync detection filter, is lengthened by 64 channel clock pulses or more.

[2] Description of CD Signal Processing-System Commands and Functions

§2-1. Description of Commands and Data Sets

$4X commands

Register name	Data 1				Data 2				Data 3			
4	Command				MAX timer value				Timer range			
	AS3	AS2	AS1	AS0	MT3	MT2	MT1	MT0	LSSL	0	0	0

Command	AS3	AS2	AS1	AS0
Cancel	0	0	0	0
Fine Search	0	1	0	RXF
Focus-On	0	1	1	1
1 Track Jump	1	0	0	RXF
10 Track Jump	1	0	1	RXF
2N Track Jump	1	1	0	RXF
M Track Move	1	1	1	RXF

RXF = 0 Forward

RXF = 1 Reverse

- When the Focus-on command ($47) is canceled, $02 is sent and the auto sequence is interrupted.
- When the Track jump commands ($44 to $45, $48 to $4D) are canceled, $25 is sent and the auto sequence is interrupted.

Cancel timer value				Timer range			
MT3	MT2	MT1	MT0	LSSL	0	0	0
23.2ms	11.6ms	5.8ms	2.9ms	0	0	0	0
1.49s	0.74s	0.37s	0.18s	1	0	0	0

- To invalidate the MAX timer, set $4X0 and the timer value to 0.

$5X commands

Timer	TR3	TR2	TR1	TR0
Blind (A, E), Overflow (C, G)	0.18ms	0.09ms	0.045ms	0.022ms
Brake (B)	0.36ms	0.18ms	0.09ms	0.045ms

$6X commands

Register name	Data 1				Data 2			
6	KICK (D)				KICK (F)			
	SD3	SD2	SD1	SD0	KF3	KF2	KF1	KF0

Timer	SD3	SD2	SD1	SD0
When executing KICK (D) $44 or $45	23.2ms	11.6ms	5.8ms	2.9ms
When executing KICK (D) $4C or $4D	11.6ms	5.8ms	2.9ms	1.45ms

Timer	KF3	KF2	KF1	KF0
KICK (F)	0.72ms	0.36ms	0.18ms	0.09ms

$7X commands

Auto sequence track jump count setting

Command	Data 1				Data 2				Data 3				Data 4			
	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4
Auto sequence track jump count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

This command is used to set N when a 2N-track jump is executed, M when an M track move is executed and the jump count when a fine search is executed for auto sequence.

- The maximum track count is 65,535, but note that with a 2N-track jump the maximum track jump count is determined by the mechanical limitations of the optical system.
- When the track jump count is from 0 to 15, the COUT signal is used to count tracks for 2N-track jump/M track move; when the count is 16 or over, the MIRR signal is used. For fine search, the COUT signal is used to count tracks.

$8X commands

Command	Data 1				Data 2			
	D19	D18	D17	D16	D15	D14	D13	D12
MODE specification	CDROM	DOUT Mute	D.out Mute-F	WSEL	VCO SEL	ASHS	SOCT	0

Command bit	C2PO timing	Processing
CDROM = 1	See the Timing Chart 2-1.	CDROM mode; average value interpolation and pre-value hold are not performed.
CDROM = 0	See the Timing Chart 2-1.	Audio mode; average value interpolation and pre-value hold are performed.

Command bit	Processing
DOUT Mute = 1	When Digital Out is on (MD2 pin = 1), DOUT output is muted.
DOUT Mute = 0	When Digital Out is on, DOUT output is not muted.

Command bit	Processing
D. out Mute F = 1	When Digital Out is on (MD2 pin = 1), DA output is muted.
D. out Mute F = 0	DA output mute is not affected when Digital Out is either on or off.

MD2	Other mute conditions*	DOUT Mute	D.out Mute F	DOUT output	DA output
0	0	0	0	off	0dB
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		–∞dB
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	0dB	0dB
1	0	0	1		–∞dB
1	0	1	0	–∞dB	0dB
1	0	1	1		–∞dB
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

* See mute conditions (1), (2) and (4) to (6) under $AX commands for other mute conditions.

Command bit	Sync protection window width	Application
WSEL = 1	±26 channel clock*	Anti-rolling is enhanced.
WSEL = 0	±6 channel clock	Sync window protection is enhanced.

* In normal-speed playback, the channel clock=4.3218MHz

Command bit	Processing	Use
VCOSEL = 0	The built-in VCO is set to normal speed.	Used for normal-speed and double-speed (double correction) playback.
VCOSEL = 1	The built-in VCO is set to high speed.	Used for quadruple-speed and double-speed (quadruple correction) playback.

Command bit	Function	Use
ASHS = 0	The command transfer rate to SSP is set to normal speed.	Used for normal-speed and double-speed (double correction) playback.
ASHS = 1	The command transfer rate to SSP is set to half speed.	Used for quadruple-speed and double-speed (quadruple correction) playback.

Command bit	Function
SOCT = 0	Sub Q is output from the SQSO pin.
SOCT = 1	Each signal is output from the SQSO pin. Input the readout clock to SQCK. (See the Timing Chart 2-11.)

$9X commands

Command	Data 1				Data 2			
	D19	D18	D17	D16	D15	D14	D13	D12
Function specification	DCLV ON-OFF	DSPB ON-OFF	A.SEQ ON-OFF	D.PLL ON-OFF	BiliGL MAIN	BiliGL SUB	FLFC	0

Command bit	CLV mode	Contents	
DCLV on/off=0	During CLVS mode	FSW = low, MON = high, MDS = Z; MDP = servo control signal, carrier frequency of 230Hz at T_B = 0 and 460Hz at T_B = 1.	
	During CLVP mode	FSW = Z, MON = high; MDS = speed control signal, carrier frequency of 7.35kHz; MDP = phase control signal, carrier frequency of 1.8kHz.	
DCLV on/off = 1 (FSW, MON not required)	During CLVS and CLVP modes	When DCLV, PWM and MD = 1	MDS = PWM polarity signal, carrier frequency of 132kHz MDP = PWM absolute value output (binary), carrier frequency of 132kHz
		When DCLV, PWM and MD = 0	MDS = Z MDP = ternary PWM output, carrier frequency of 132kHz

When DCLV on/off = 1 for the Digital CLV servo, the sampling frequency of the internal digital filter switches simultaneously with the CLVP/CLVS switching.

Therefore, the cut-off frequency for the CLVS is fc = 70Hz at T_B = 0, and fc = 140Hz at T_B = 1.

Command bit	Processing
DSPB = 0	Normal-speed playback, C2 error quadruple correction, variable pitch possible.
DSPB = 1	Double-speed playback, C2 error double correction, variable pitch prohibited.

Normally, FLFC is 0.

Command bit	Meaning
DPLL = 0*	RFPLL is analog. PDO, VCOI and VCOO are used.
DPLL = 1	RFPLL is digital. PDO is high impedance.

* External parts for Pins 18 to 20 are required even when analog PLL is selected.

Command bit	BiliGL MAIN = 0	BiliGL MAIN = 1
BiliGL SUB = 0	STEREO	MAIN
BiliGL SUB = 1	SUB	Mute

Definition of bilingual capable MAIN, SUB and STEREO

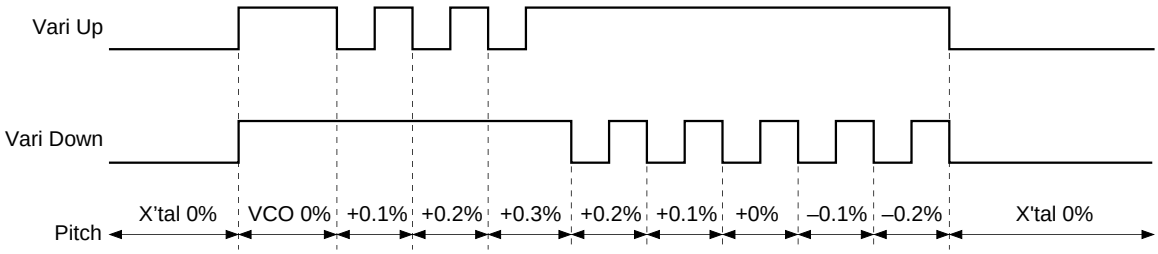
The left channel input is output to the left and right channels for MAIN.

The right channel input is output to the left and right channels for SUB.

The left and right channel inputs are output to the left and right channels for STEREO.

$AX commands

Command	Data 1				Data 2			
	D19	D18	D17	D16	D15	D14	D13	D12
Audio CTRL	Vari Up	Vari Down	Mute	ATT	PCT1	PCT2	0	0



Command bit	Meaning
Mute = 0	Mute off if other mute conditions are not set.
Mute = 1	Mute on. Peak register reset.

Command bit	Meaning
ATT = 0	Attenuation off
ATT = 1	–12dB

Mute conditions

(1) When register A mute = 1.
(2) When Mute pin = 1.
(3) When register 8 D.out Mute F = 1 and the Digital Out is on (MD2 pin = 1).
(4) When GFS stays low for over 35ms (during normal-speed).
(5) When register 9 BiliGL MAIN = Sub = 1.
(6) When register A PCT1 = 1 and PCT2 = 0.

(1) to (4) perform zero-cross muting with a 1 ms time limit.

Command bit		Meaning	PCM Gain	ECC error correction ability
PCT1	PCT2			
0	0	Normal mode	× 0dB	C1: double; C2: quadruple
0	1	Level meter mode	× 0dB	C1: double; C2: quadruple
1	0	Peak meter mode	Mute	C1: double; C2: double
1	1	Normal mode	× 0dB	C1: double; C2: double

Description of level meter mode (see the Timing Chart 2-2.)

- When the LSI is set to this mode, it can possess digital level meter functions.
- When the 96-bit clock is input to SQCK, 96 bits of data are output to SQSO.
  The initial 80 bits of data are Sub Q data (see §2-2. Subcode Interface). The last 16 bits are LSB first, 15-bit PCM data (absolute values).
  The final bit is PCM data. However, it is high when generated by the left channel and low when generated by the right channel.
- PCM data is reset and the L/R flag is reversed after one readout.
  The maximum value for this status is then measured until the next readout.

Description of peak meter mode (see the Timing Chart 2-3.)

- When the LSI is set to this mode, the maximum PCM data value is detected regardless of if it comes from the left or right channel.
  The 96-bit clock must be input to SQCK to read out this data.
- When the 96-bit clock is input, 96 bits of data are output to SQSO and the LSI internal register is reset.
  In other words, the PCM maximum value detection register is not reset by the readout.
- To reset the PCM maximum value detection register, set PCT1 = PCT2 = 0 or set the $AX mute.
- The Sub Q absolute time is automatically controlled in this mode.
  In other words, after the maximum value is generated, the absolute time for CRC to become OK is retained in the memory. The normal operation is conducted for the relative time.
- The final bit (L/R flag) of the 96-bit data is normally 0.
- The pre-value hold and average value interpolation data are fixed to level (–∞) for this mode.

$BX commands

This command sets the traverse monitor count.

Command	Data 1				Data 2				Data 3				Data 4			
	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4
Traverse monitor count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

- When the set number of tracks are counted during fine search, the sled control for the traverse cycle control goes off.
- The traverse monitor count is set when the traverse status is monitored by the SENS output COMP and COUT.

$CX commands

Command	Data 1				Data 2				Explanation
	D19	D18	D17	D16	D15	D14	D13	D12	
Servo coefficient setting	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	0	Gain DCLV0	0	0	Valid only when DCLV = 1.
CLV CTRL ($DX)				Gain CLVS					Valid when DCLV = 1 or 0.

The spindle servo gain is externally set when DCLV = 1.

- CLVS mode gain setting: GCLVS

Gain MDS1	Gain MDS0	Gain CLVS	GCLVS
0	0	0	–12dB
0	0	1	–6dB
0	1	0	–6dB
0	1	1	0dB
1	0	0	0dB
1	0	1	+6dB

Note) When DCLV = 0, the CLVS gain is as follows:
When Gain CLVS = 0, GCLVS = –12dB.
When Gain CLVS = 1, GCLVS = 0dB.

• CLVP mode gain setting: GMDP: GMDS

Gain MDP1	Gain MDP0	GMDP
0	0	–6dB
0	1	0dB
1	0	+6dB

Gain MDS1	Gain MDS0	GMDS
0	0	–6dB
0	1	0dB
1	0	+6dB

• DCLV overall gain setting: GDCLV

Gain DCLV0	GDCLV
0	0dB
1	+6dB

$DX commands

Command	D19	D18	D17	D16
CLV CTRL	DCLV PWM MD	TB	TP	Gain CLVS

See the $CX commands.

Command bit	Explanation (See the Timing Chart 2-4.)
DCLV PWM MD = 1	Digital CLV PWM mode specified. Both MDS and MDP are used.
DCLV PWM MD = 0	Digital CLV PWM mode specified. Ternary MDP values are output.

Command bit	Explanation
TB = 0	Bottom hold in CLVS and CLVH modes at a cycle of RFCK/32.
TB = 1	Bottom hold in CLVS and CLVH modes at a cycle of RFCK/16.
TP = 0	Peak hold in CLVS mode at a cycle of RFCK/4.
TP = 1	Peak hold in CLVS mode at a cycle of RFCK/2.

Note) Peak hold is performed at 34kHz in CLVH mode.

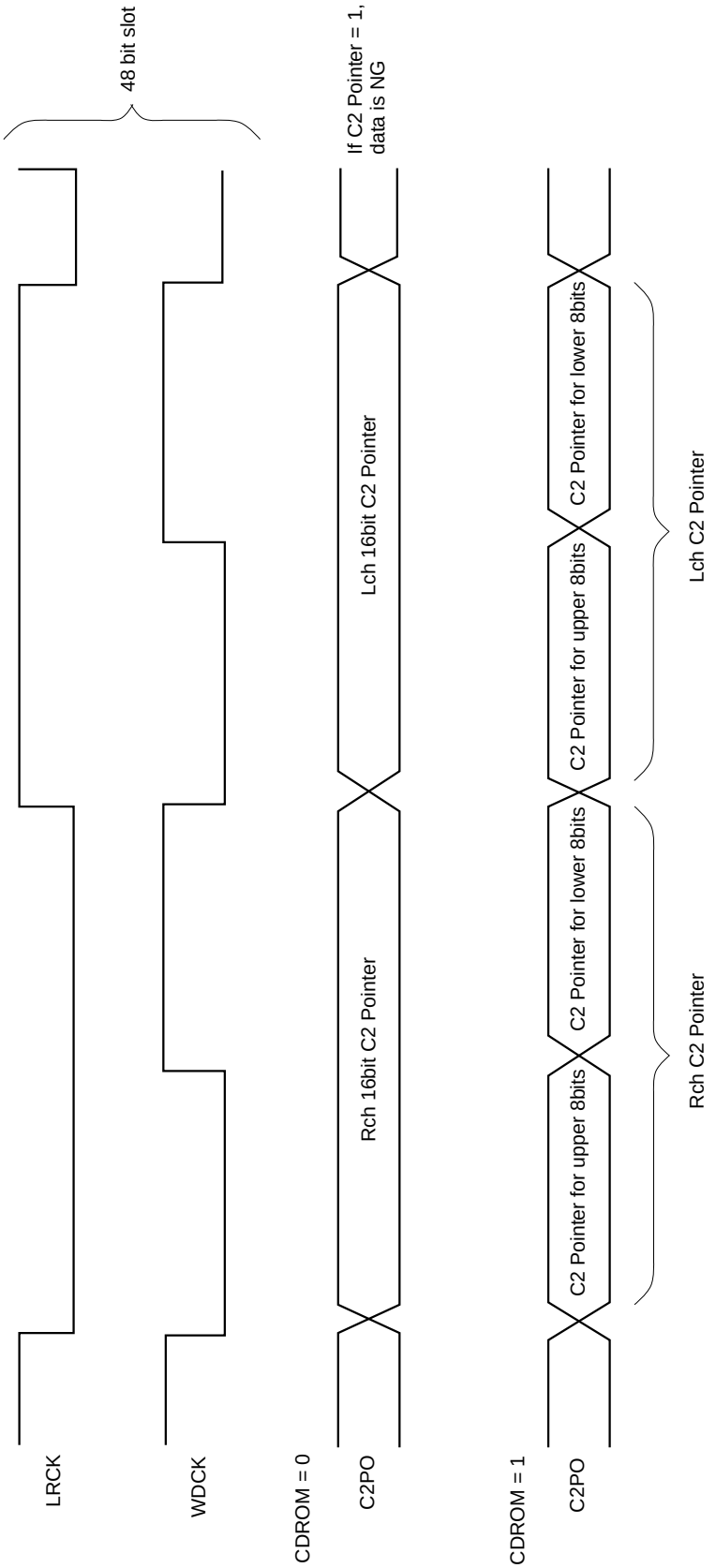
$EX commands

Command	D19	D18	D17	D16
CLV mode	CM3	CM2	CM1	CM0

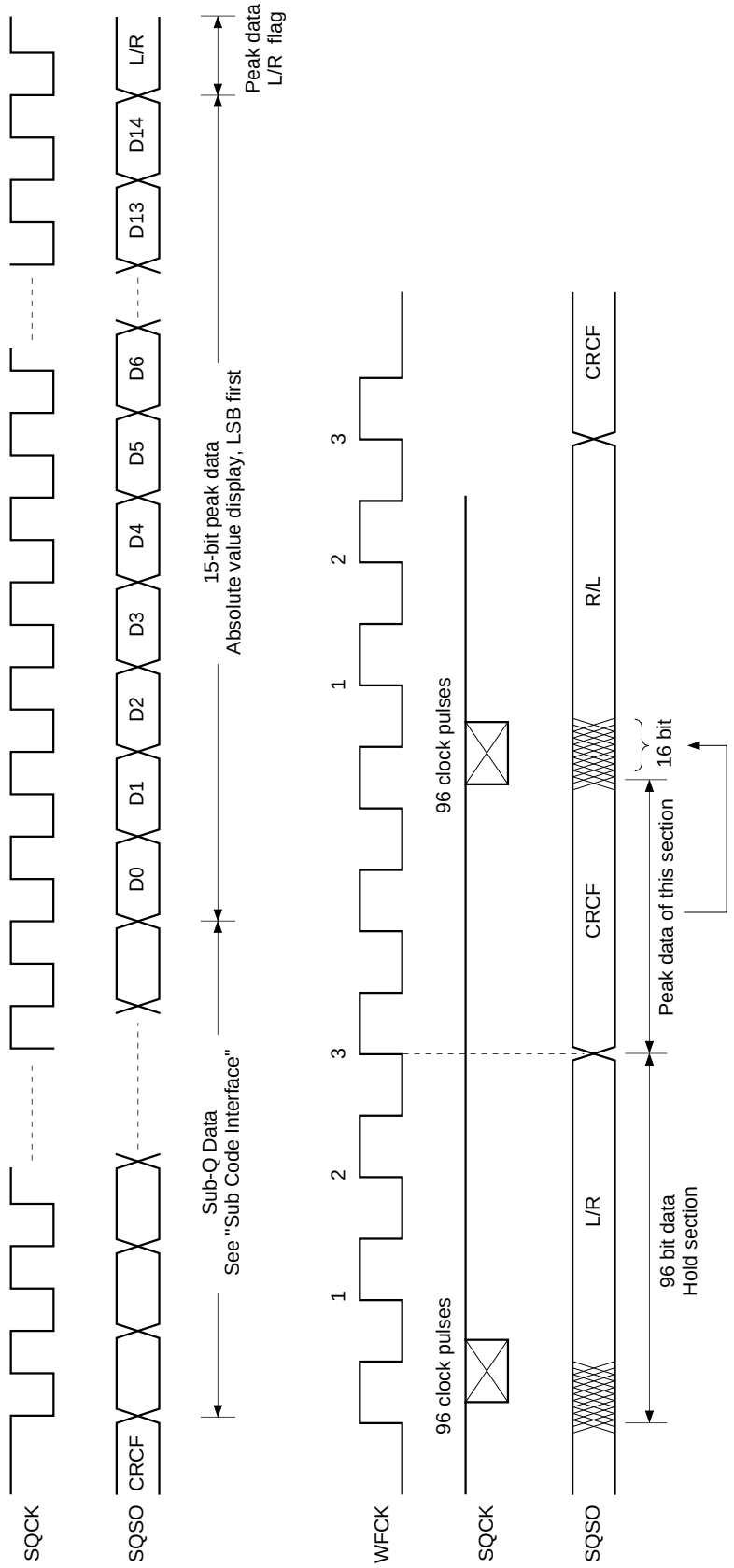
CM3	CM2	CM1	CM0	Mode	Explanation
0	0	0	0	STOP	See the Timing Chart 2-5.
1	0	0	0	KICK	See the Timing Chart 2-6.
1	0	1	0	BRAKE	See the Timing Chart 2-7.
1	1	1	0	CLVS	
1	1	0	0	CLVH	
1	1	1	1	CLVP	
0	1	1	0	CLVA	

STOP: Spindle motor stop mode
KICK: Spindle motor forward rotation mode
BRAKE: Spindle motor reverse rotation mode
CLVS: Rough servo mode. When the RF-PLL circuit lock is disengaged, this mode is used to pull the disc rotations within the RF-PLL capture range.
CLVP: PLL servo mode
CLVA: Automatic CLVS/CLVP switching mode. This mode is normally used during playback.

Timing Chart 2-1

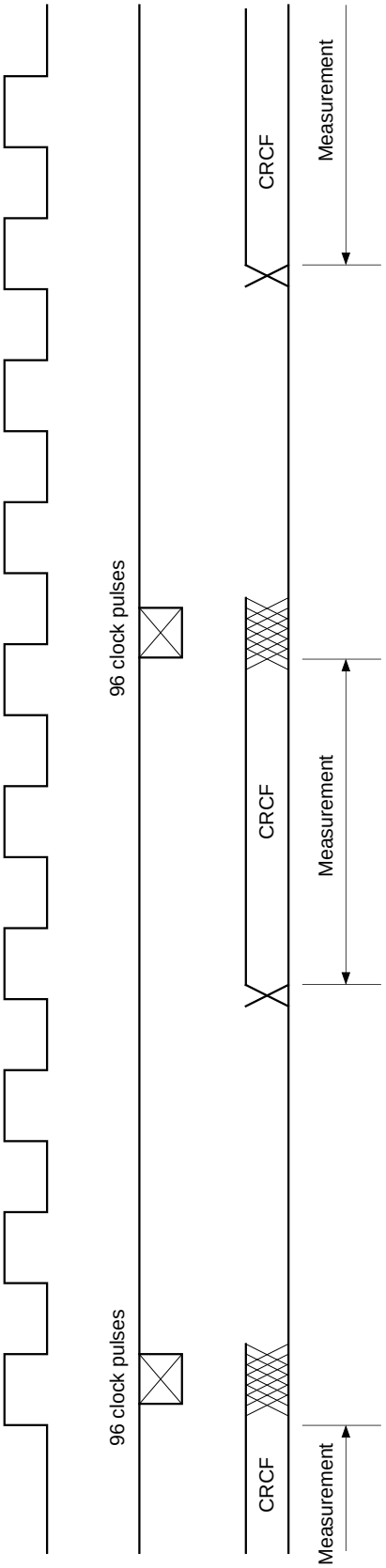


Timing Chart 2-2



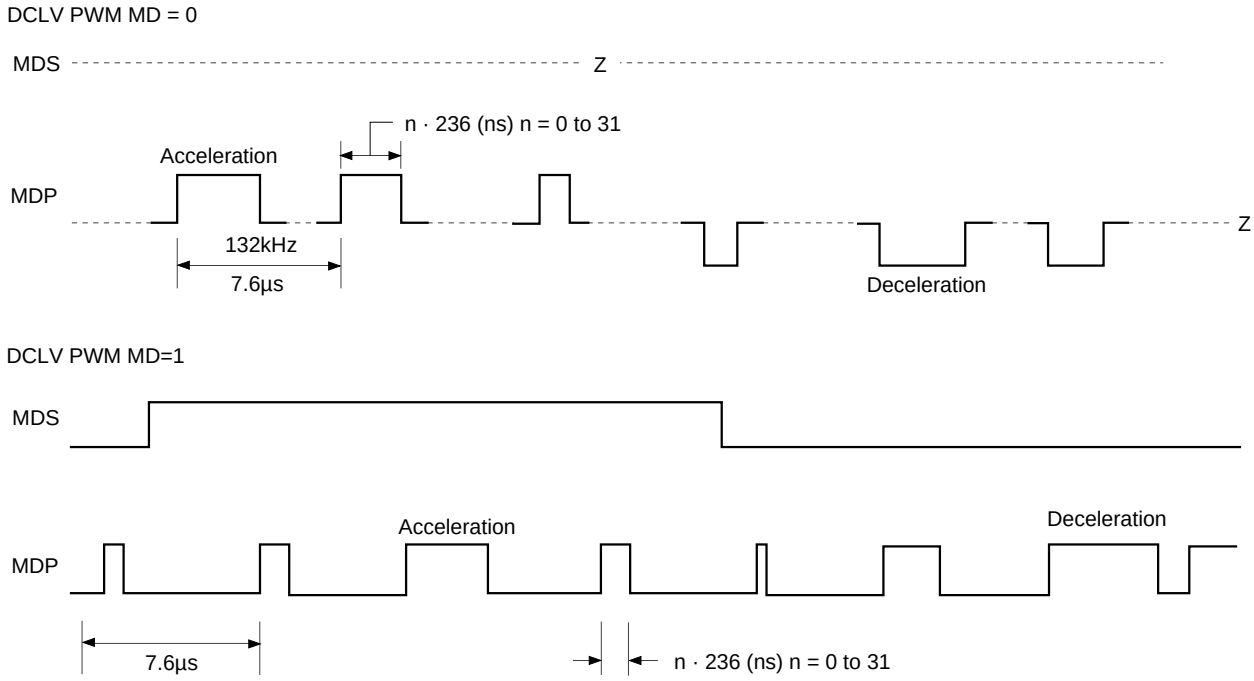
Level Meter Timing

Timing Chart 2-3



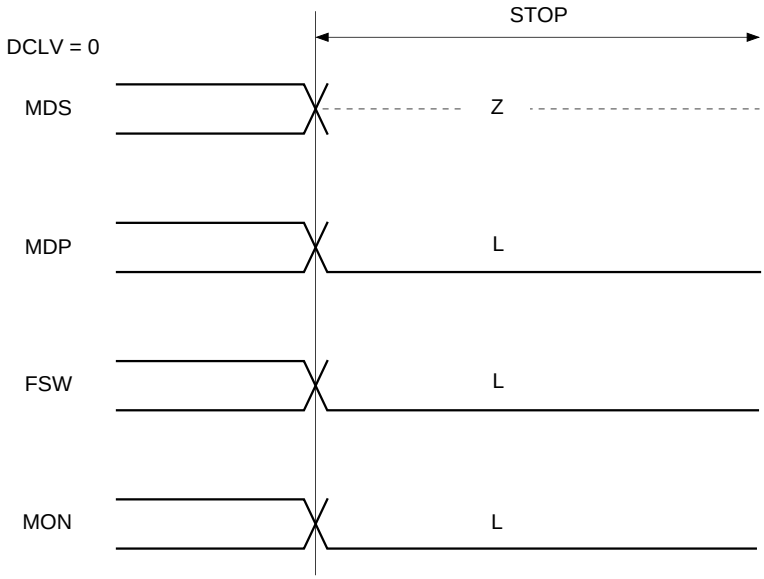
Peak Meter Timing

Timing Chart 2-4

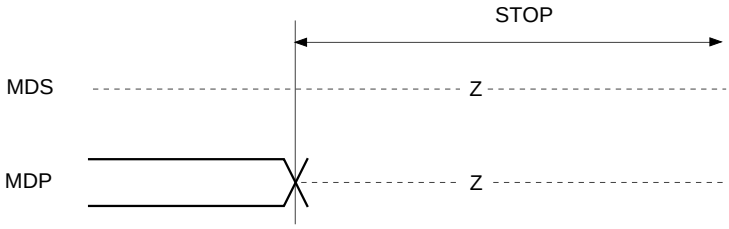


Output Waveforms with DCLV = 1

Timing Chart 2-5

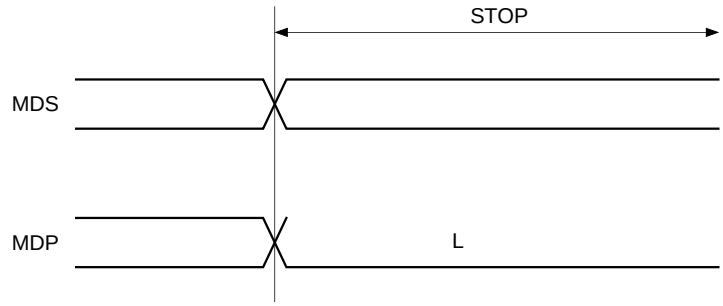


DCLV = 1 DCLV PWM MD = 0



FSW and MON are the same as for DCLV = 0

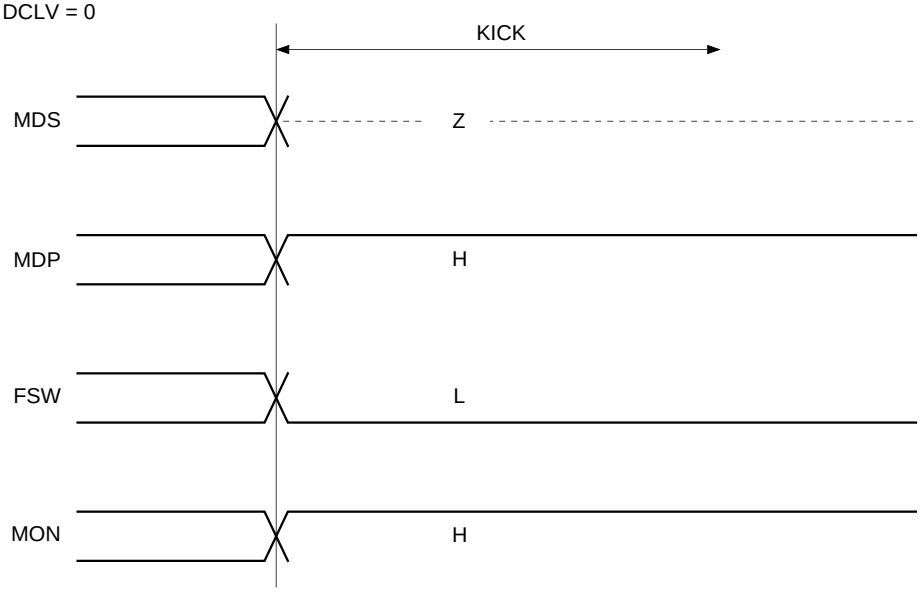
DCLV = 1 DCLV PWM MD = 1



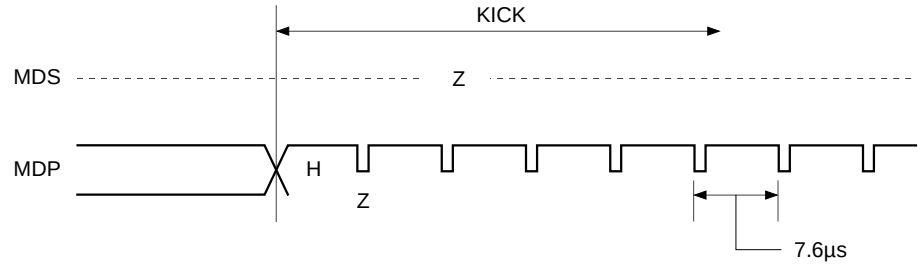
FSW and MON are the same as for DCLV = 0

Timing Chart 2-6

DCLV = 0

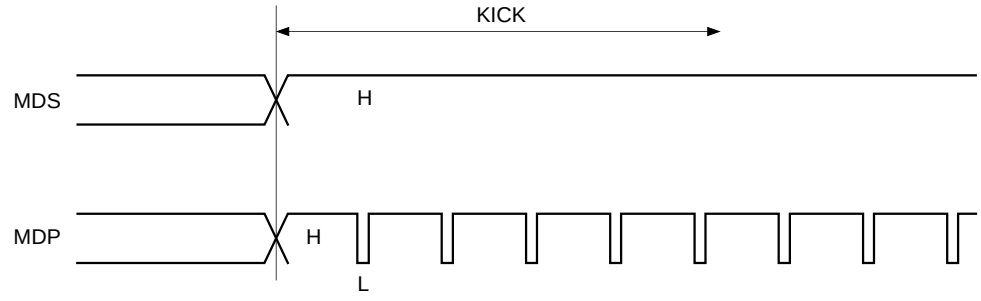


DCLV = 1 DCLV PWM MD = 0



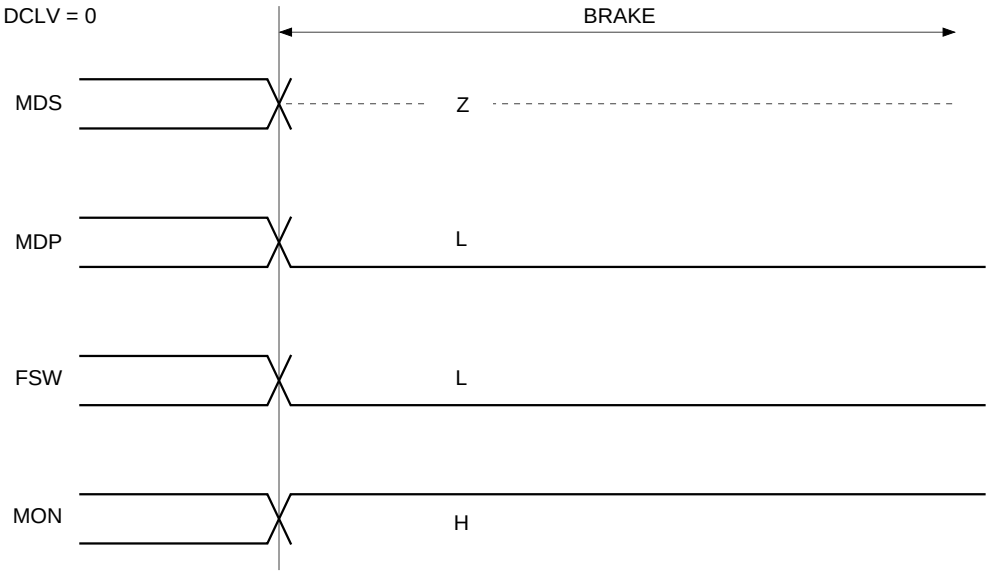
FSW and MON are the same as for DCLV = 0

DCLV = 1 DCLV PWM MD = 1

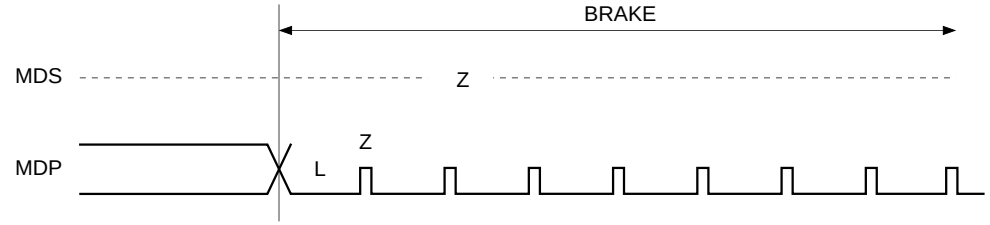


FSW and MON are the same as for DCLV = 0

Timing Chart 2-7

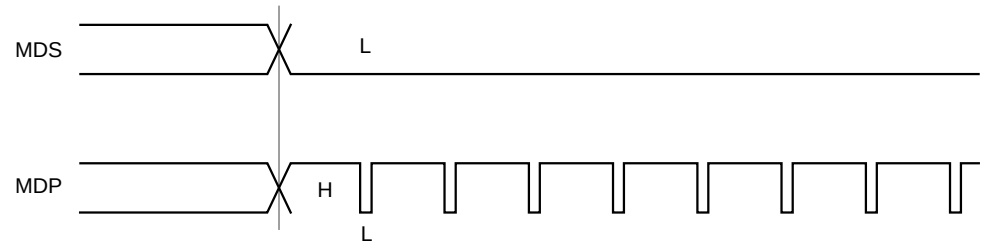


DCLV = 1 DCLV PWM MD = 0



FSW and MON are the same as for DCLV = 0

DCLV = 1 DCLV PWM MD = 1



FSW and MON are the same as for DCLV = 0

§2-2. Subcode Interface

This section explains the subcode interface.
There are two methods for reading out a subcode externally. The 8-bit subcodes P to W can be read from SBSO by inputting EXCK.
Sub Q can be read out after the CRC check of the 80 bits of information in the subcode frame.
This is accomplished, after checking SCOR and CRCF, by inputting 80 clock pulses to SQCK and reading data from the SQSO pin.

P to W Subcode Read

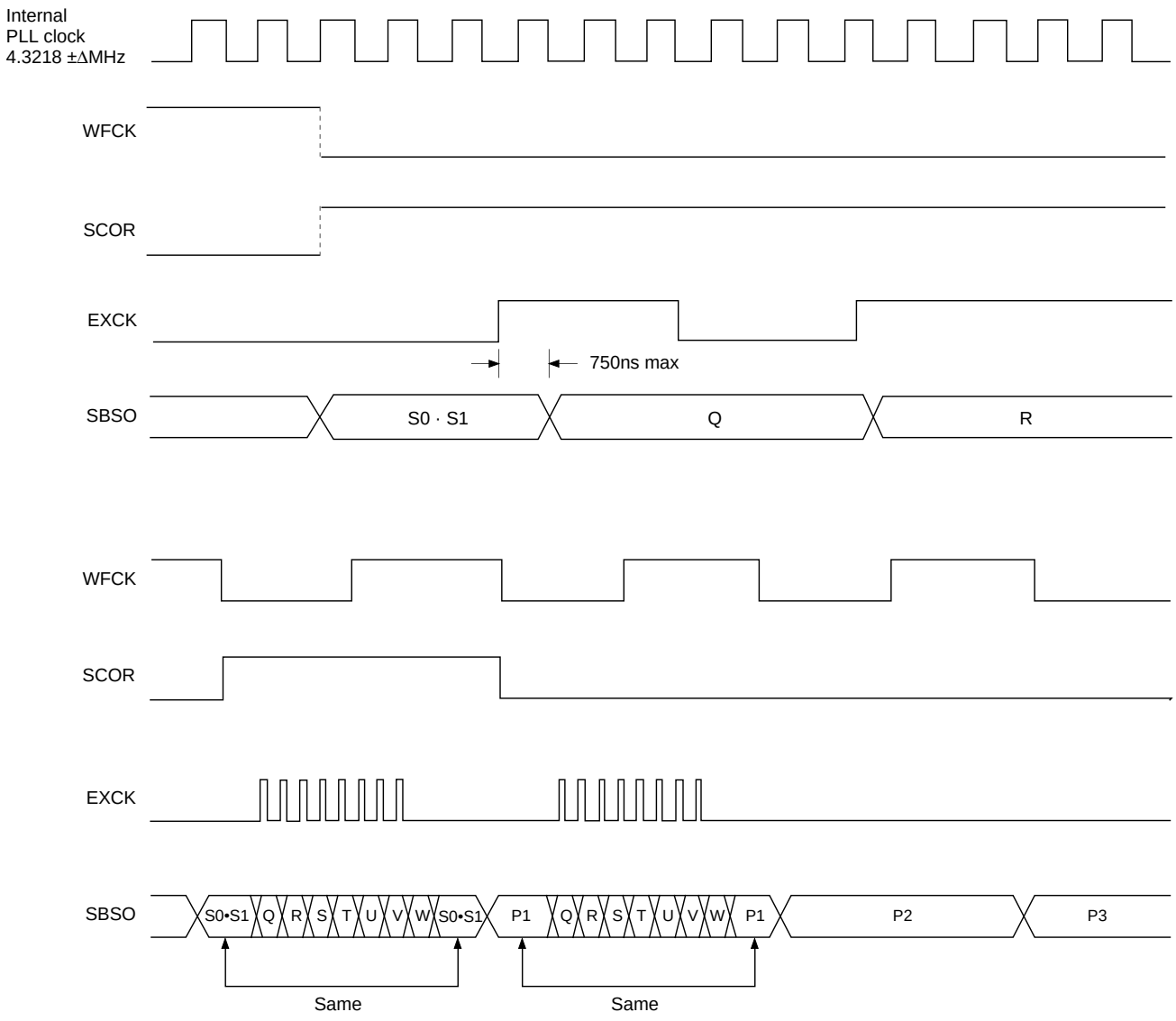
Data can be read out by inputting EXCK immediately after WFCK falls. (See the Timing Chart 2-8.)

80-bit Sub Q Read

Fig. 2-9 shows the peripheral block of the 80-bit Sub Q register.

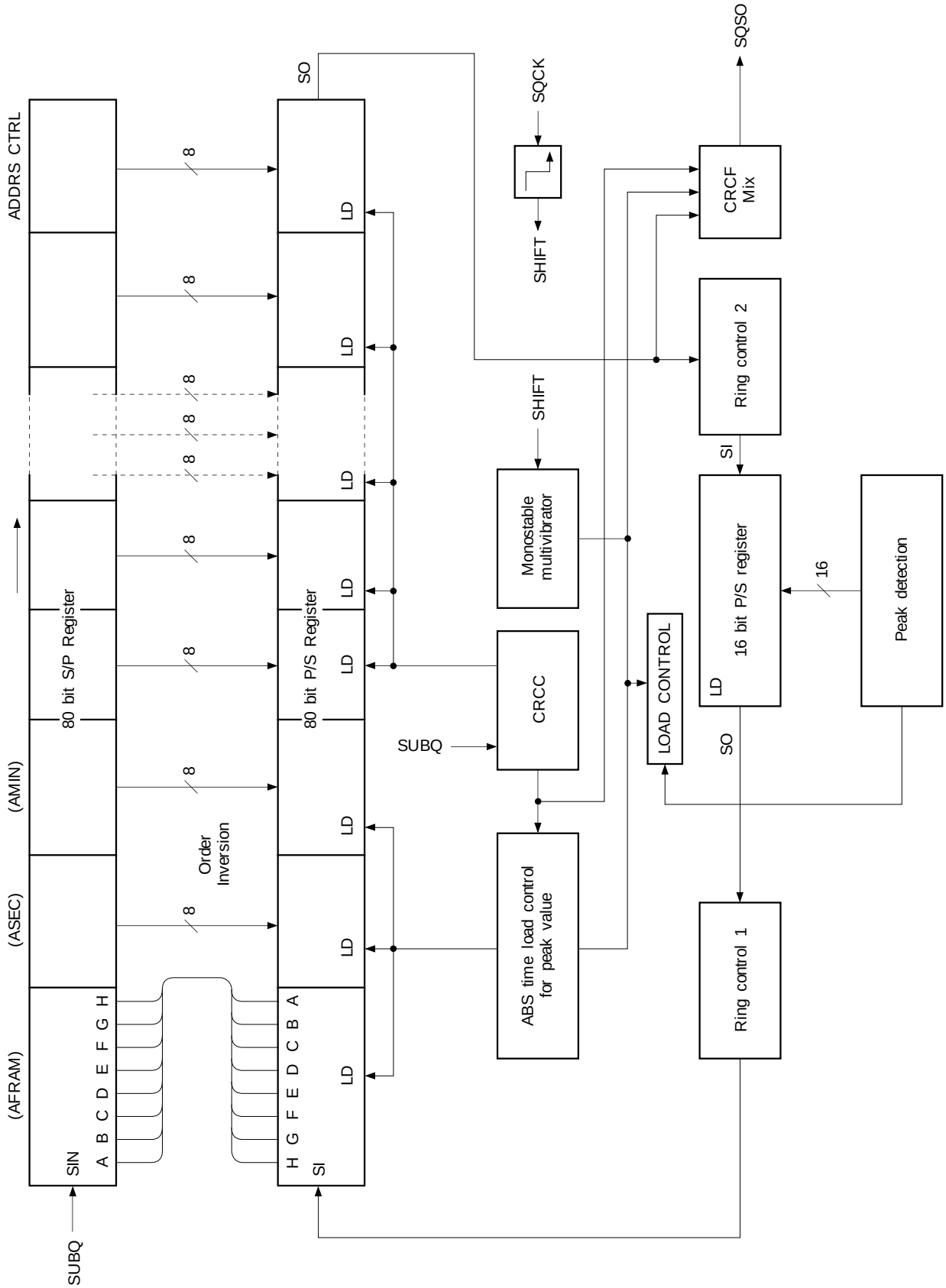
- First, Sub Q, regenerated at one bit per frame, is input to the 80-bit serial/parallel register and the CRC check circuit.
- 96-bit Sub Q is input, and if the CRC is OK, it is output to SQSO with CRCF = 1. In addition, the 80 bits are loaded into the parallel/serial register.
  When SQSO goes high after SCOR is output, the CPU determines that new data (which passed the CRC check) has been loaded.
- In the CXD2545Q, when 80-bit data is loaded, the order of the MSB and LSB is inverted for each byte. As a result, although the sequence of the bytes is the same, the bits within the bytes are now ordered LSB first.
- Once the fact that the 80-bit data has been loaded is confirmed, SQCK is input so that the data can be read. In this LSI, the SQCK input is detected, and the retriggerable monostable multivibrator for low is reset.
- The retriggerable monostable multivibrator has a time constant from 270 to 400µs. When the duration when SQCK is high is less than this time constant, the monostable multivibrator is kept reset; during this interval, the S/P register is not loaded into the P/S register.
- While the monostable multivibrator is being reset, data cannot be loaded into the peak detection parallel/serial register or the 80-bit parallel/serial register.
  In other words, while reading out with a clock cycle shorter than the monostable multivibrator time constant, the register will not be rewritten by CRCOK and others.
- In this LSI, the previously mentioned peak detection register can be connected to the shift-in of the 80-bit P/S register.
  Input and output for ring control 1 are shorted in peak meter or level meter mode.
  Those for ring 2 are shorted in peak meter mode.
  This is because the register is reset with each readout in level meter mode, and to prevent readout destruction in peak meter mode.
  As a result, the 96-bit clock must be input in peak meter mode.
- In addition, as previously mentioned, the absolute time after peak is generated is stored in the memory in peak meter mode. (See the Timing Chart 2-10.)
- Although a clock is input from the SQCK pin to actually perform these operations, the high and low intervals for this clock should be between 750ns and 120µs.

Timing Chart 2-8

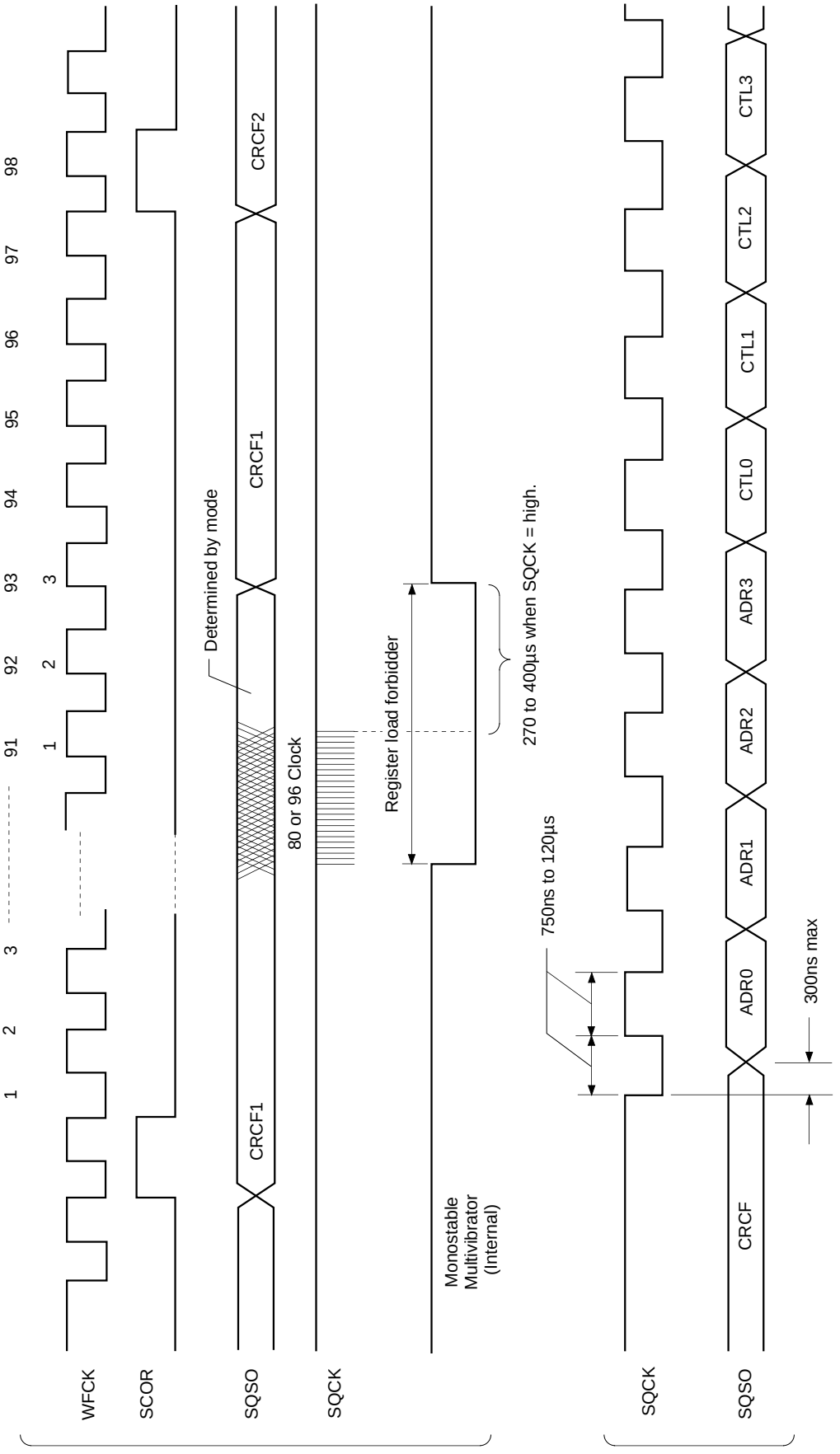


Subcode P.Q.R.S.T.U.V.W Read Timing

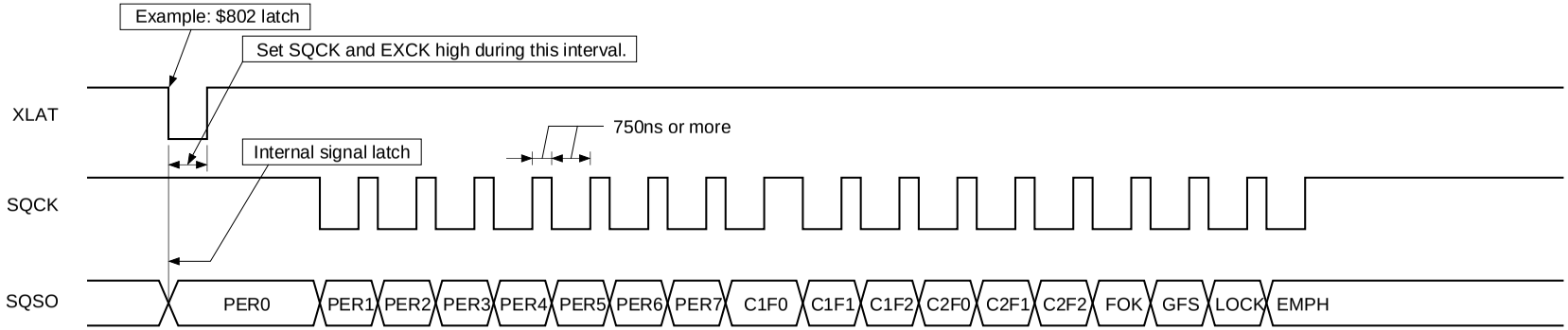
Block Diagram 2-9



Timing Chart 2-10



Timing Chart 2-11



Signal	Explanation
PER0 to PER7*	RF jitter amount (used to adjust the focus bias). 8-bit binary data in PER0 = LSB, PER7 = MSB.
FOK	Focus OK
GFS	High when the frame sync and the insertion protection timing match.
LOCK	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low.
EMPH	Outputs a high signal when the playback disc has emphasis.

* RF jitter amount PER0 to PER7 are output in binary code. When the RF jitter amount is small, the correlation is such that the binary code number decreases.

C1F2	C1F1	C1F0	Description	
0	0	0	No C1 errors;	C1 pointer reset
0	0	1	One C1 error corrected;	C1 pointer reset
0	1	0	—	
0	1	1	—	
1	0	0	No C1 errors;	C1 pointer set
1	0	1	One C1 error corrected;	C1 pointer set
1	1	0	Two C1 errors corrected;	C1 pointer set
1	1	1	C1 correction impossible;	C1 pointer set

C2F2	C2F1	C2F0	Description	
0	0	0	No C2 errors;	C2 pointer reset
0	0	1	One C2 error corrected;	C2 pointer reset
0	1	0	Two C2 errors corrected;	C2 pointer reset
0	1	1	Three C2 errors corrected;	C2 pointer reset
1	0	0	Four C2 errors corrected;	C2 pointer reset
1	0	1	—	
1	1	0	C2 correction impossible;	C1 pointer copy
1	1	1	C2 correction impossible;	C2 pointer set

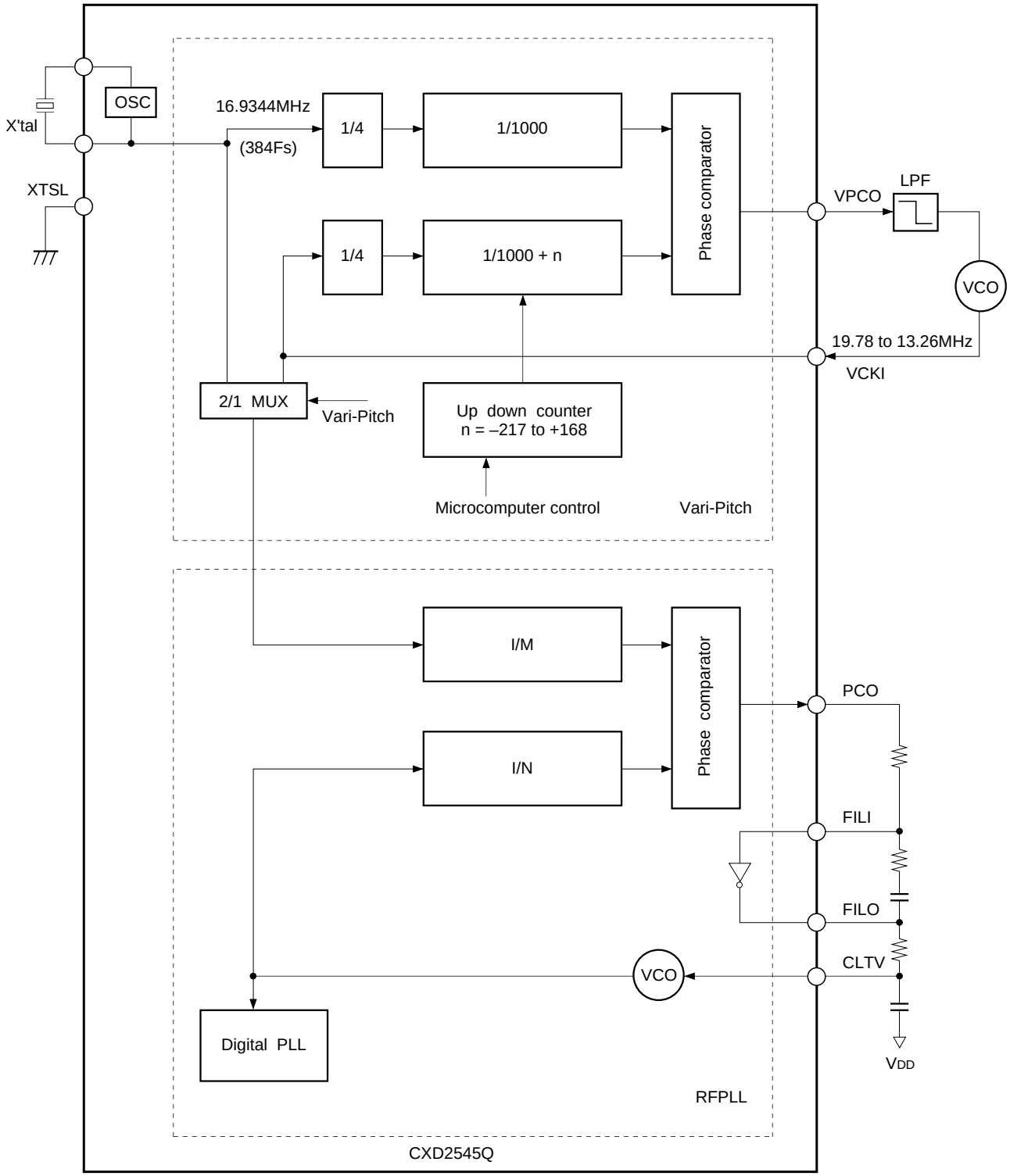
§2-3. Digital PLL

- The channel clock is necessary for demodulating the EFM signal regenerated by the optical system.
  Assuming T as the channel clock cycle, the EFM signal is modulated in an integer multiple of T from 3T to 11T. In order to read the information in the EFM signal, this integer value must be read correctly. As a result, T, that is the channel clock, is necessary.
  In an actual player, PLL is necessary to regenerate the channel clock because the fluctuation in the spindle rotation alters the width of the EFM signal pulses.

The block diagram of this PLL is shown in Fig. 2-12.
The CXD2545Q has a built-in three-stage PLL.

- The first-stage PLL regenerates the variable pitch.
  LPF and VCO are necessary as external parts.
  The minimum variable amount of pitch is 0.1%. The output of this first-stage PLL is used as a reference for all clocks within the LSI. Input the XTAO output to the VCKI pin when variable pitch is not used.
- The second-stage PLL regenerates a high-frequency clock needed by the third-stage digital PLL.
- The third-stage PLL is a digital PLL that regenerates the actual channel clock, and has a ±150kHz (normal-speed playback) or more capture range.

Block Diagram 2-12



§2-4. EFM Frame Sync Protection

- In a CD player operating at normal speed, a frame sync is recorded approximately every 136µs (7.35kHz). This signal is used as a reference to know which data is the data within a frame. Conversely, if the frame sync cannot be recognized, the data is processed as error data because the data cannot be recognized. As a result, recognizing the frame sync properly is extremely important for improving playability.
- In the CXD2545Q, window protection and forward protection/backward protection have been adopted for frame sync protection. The adoption of these functions achieves very powerful frame sync protection.
  There are two window widths; one for cases where a rotational disturbance affects the player and the other for cases where there is no rotational disturbance (WSEL = 0/1). In addition, the forward protection counter is fixed to 13, and the backward protection counter to 3. In other words, when the frame sync is being regenerated normally and then cannot be detected due to scratches, a maximum of 13 frames are inserted. If the frame sync cannot be detected for 13 frames or more, the window is released and the frame sync is resynchronized.
  In addition, immediately after the window is released and the resynchronization is executed, if a proper frame sync cannot be detected within 3 frames, the window is released immediately.

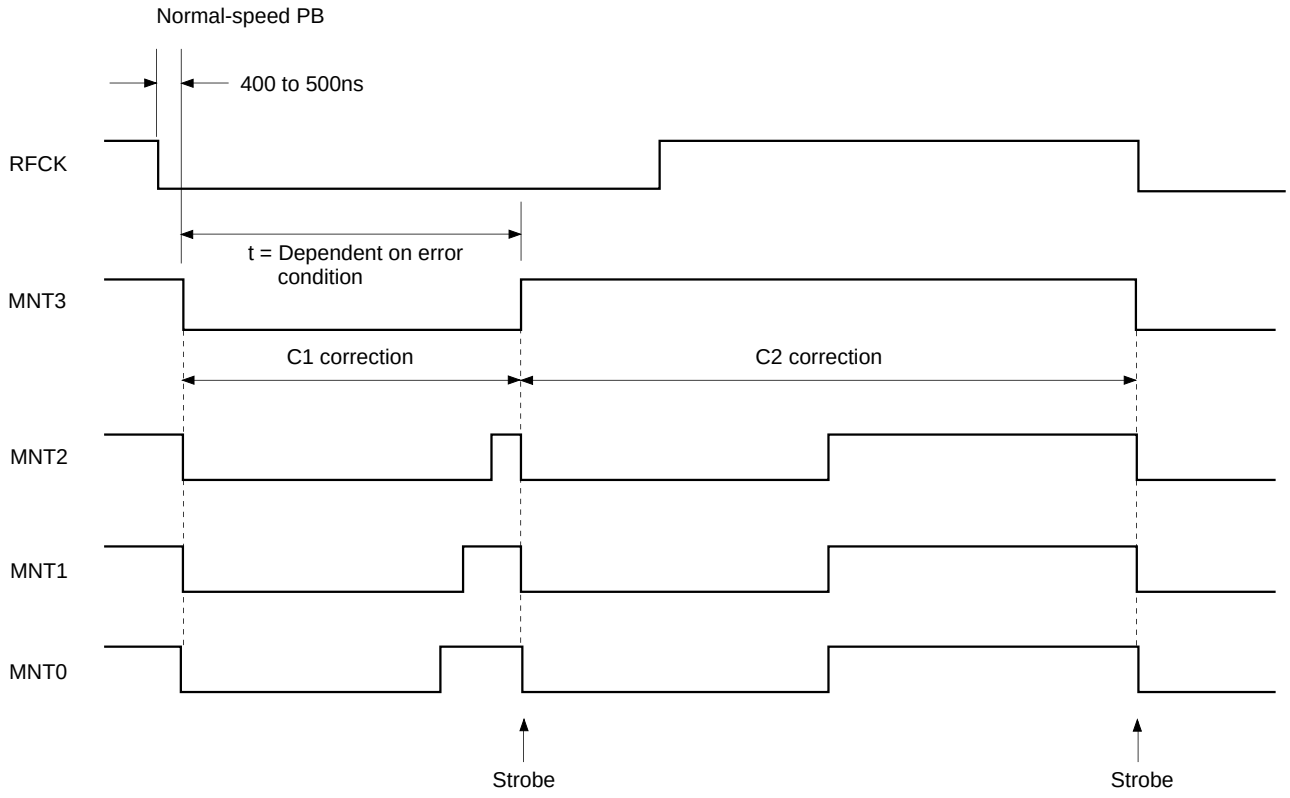
§2-5. Error Correction

- In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity.
  For C2 correction, the code is created with 24-byte information and 4-byte C2 parity.
  Both C1 and C2 are Reed Solomon codes with a minimum distance of 5.
- The CXD2545Q uses refined super strategy to achieve double correction for C1 and quadruple correction for C2.
- In addition, to prevent C2 miscorrection, a C1 pointer is attached to data after C1 correction according to the C1 error status, the generation status of the EFM signal, and the operating status of the player.
- The correction status can be monitored outside the LSI. See the Table 2-13.
- When the C2 pointer is high, the data in question was uncorrectable.
  Either the pre-value was held or an average value interpolation was made for the data.

MNT3	MNT2	MNT1	MNT0	Description
0	0	0	0	No C1 errors; C1 pointer reset
0	0	0	1	One C1 error corrected; C1 pointer reset
0	0	1	0	—
0	0	1	1	—
0	1	0	0	No C1 errors; C1 pointer set
0	1	0	1	One C1 error corrected; C1 pointer set
0	1	1	0	Two C1 errors corrected; C1 pointer set
0	1	1	1	C1 correction impossible; C1 pointer set
1	0	0	0	No C2 errors; C2 pointer reset
1	0	0	1	One C2 error corrected; C2 pointer reset
1	0	1	0	Two C2 errors corrected; C2 pointer reset
1	0	1	1	Three C2 errors corrected; C2 pointer reset
1	1	0	0	Four C2 errors corrected; C2 pointer reset
1	1	0	1	—
1	1	1	0	C2 correction impossible; C1 pointer copy
1	1	1	1	C2 correction impossible; C2 pointer set

Table 2-13.

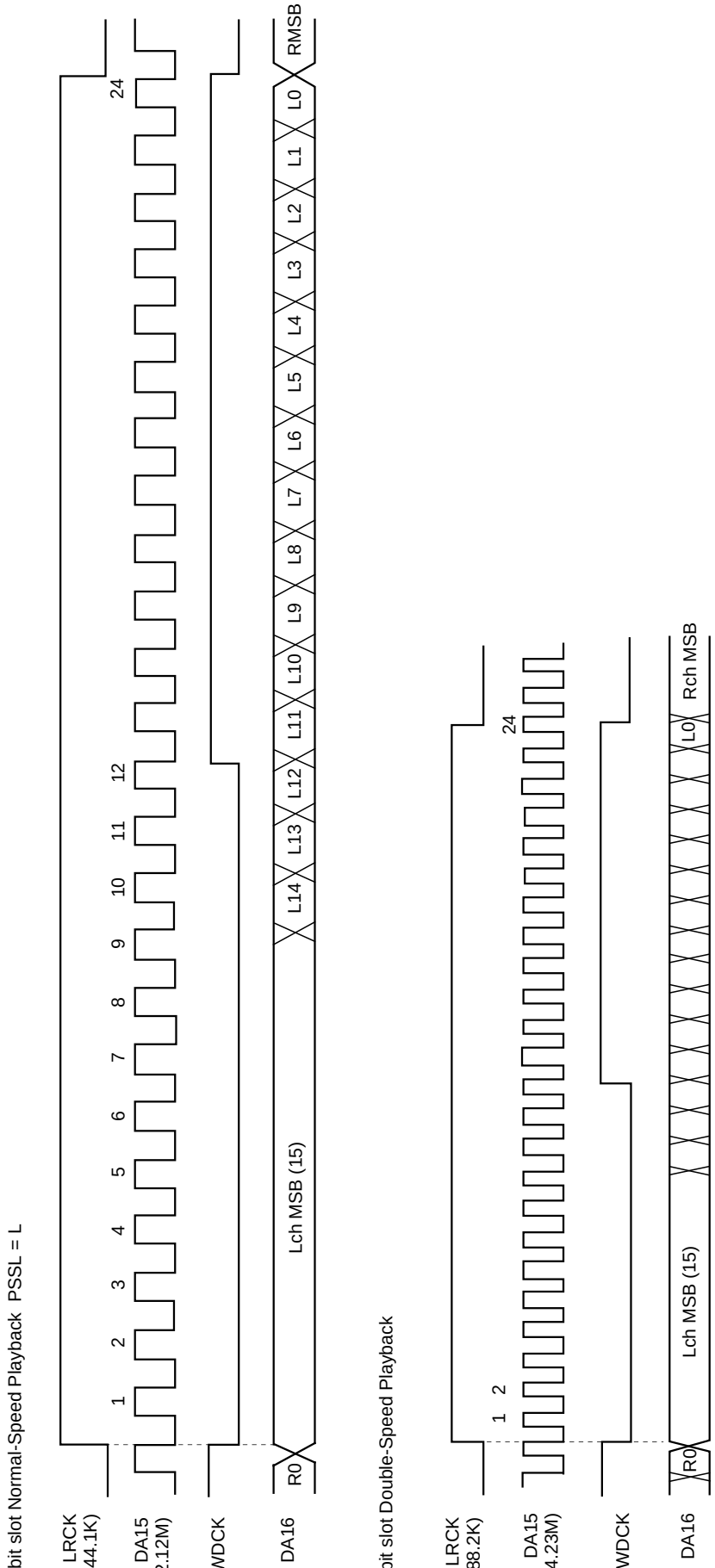
Timing Chart 2-14



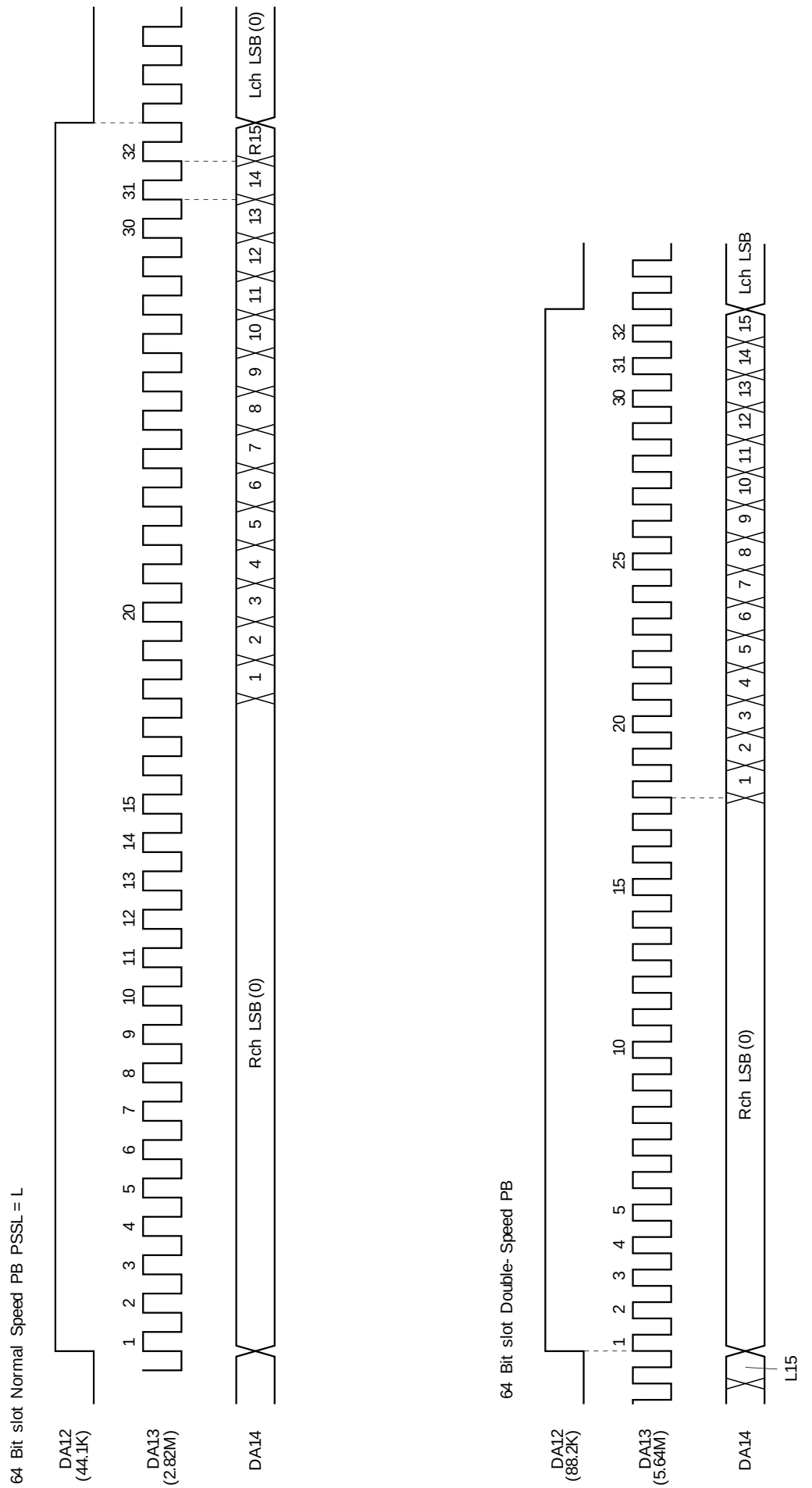
§2-6. DA Interface

- The CXD2545Q has two modes as DA interfaces.
  a) 48-bit slot interface
     This interface includes 48 cycles of the bit clock within one LRCK cycle, and is MSB first.
     When LRCK is high, the data is for the left channel.
  b) 64-bit slot interface
     This interface includes 64 cycles of the bit clock within one LRCK cycle, and is LSB first.
     When LRCK is low, the data is for the left channel.

Timing Chart 2-15



Timing Chart 2-16



§2-7. Digital Out

There are three digital output formats; the type 1 format for broadcasting stations, the type 2 form 1 format for home use, and the type 2 form 2 format for the manufacture of software.
The CXD2545Q supports Type 2 form 1.
Regarding the clock accuracy of the channel status, level III is set automatically when the crystal clock is used and level II is variable pitch. In addition, Sub Q data which are matched twice in succession after a CRC check are input to the first four bits (bits 0 to 3).
DOUT is output when the crystal is 34 MHz, the variable pitch is reset, and DSPB = 1. Therefore, set MD2 to 0 and turn DOUT off.

Digital Out C bit

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	From sub-Q				0	0	0	0	1	0	0	0	0	0	0	0
	ID0	ID1	COPY	Emph												
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0
32																
48								0								
176																

bit0 to 3 .....Sub Q control bits that matched twice with CRCOK
bit29 .....Varipitch: 1 X'tal: 0

Table 2-17.

§2-8. Servo Auto Sequence

This function performs a series of controls, including auto focus and track jumps. When the auto sequence command is received from the CPU, auto focus, 1 track jump, 2N track jumps, fine search, and M track move are executed automatically.
The servo block is used in an exclusive manner during the auto sequence execution (when XBUSY = low), so that commands from the CPU are not transferred to the servo block, but can be sent to the signal processor block.
In addition, when using the auto sequencer, turn the A.SEQ of register 9 on.
When the clock goes from low to high while XBUSY is low, XBUSY does not become high for a maximum of 100µs after that point. This is designed to prevent the transfer of erroneous data to the servo block when XBUSY changes from low to high by the monostable multivibrator, which is reset by CLOK being low (When XBUSY is low).

In addition, a MAX timer is built-in as a countermeasure against abnormal operation due to external disturbances, etc. When the auto sequence command is sent from the CPU, this command assumes a $4XY format, in which X specifies the command and Y sets the MAX timer value and timer range. If the executed auto sequence command does not terminate within the set timer value, the auto sequence is interrupted (like $40). See 2-1, $4X commands concerning the timer value and range. Also, the MAX timer is invalidated by inputting $4X0.
Although this command is explained in the format of $4X in the following command descriptions, the timer value and timer range should be actually sent together from the CPU.

(a) Auto focus ($47)

Focus search-up is performed, FOK and FZC are checked, and the focus servo is turned on.

If $47 is received from the CPU, the focus servo is turned on according to Fig. 2-18. The auto focus is executed after focus search-up, and the pickup should be lowered beforehand (focus search-down). In addition, blind E of register 5 is used to eliminate FZC chattering. In other words, the focus servo is turned on at the falling edge of FZC after FZC has been continuously high for a longer time than E.

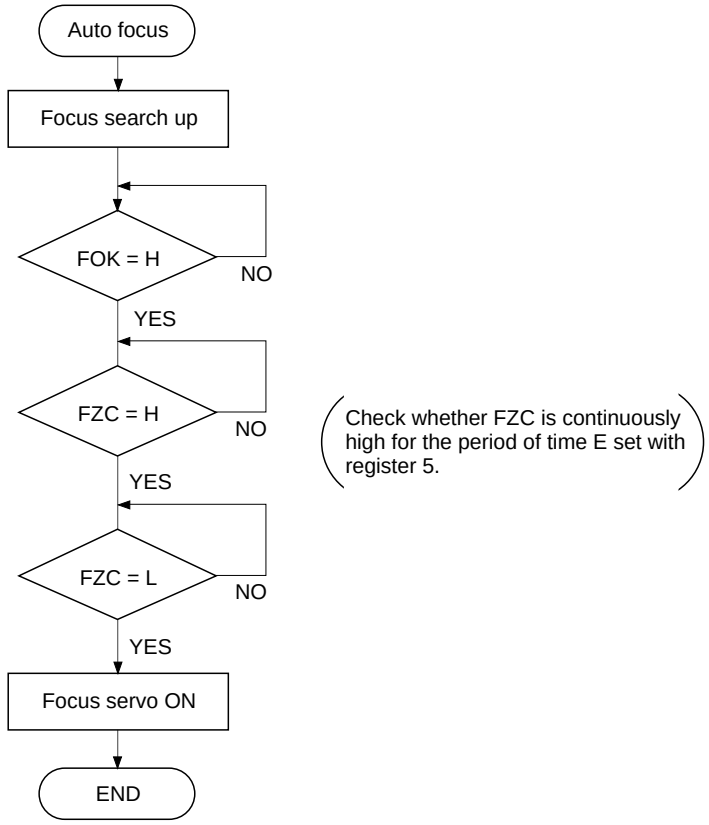


Fig. 2-18 (a). Auto Focus Flow Chart

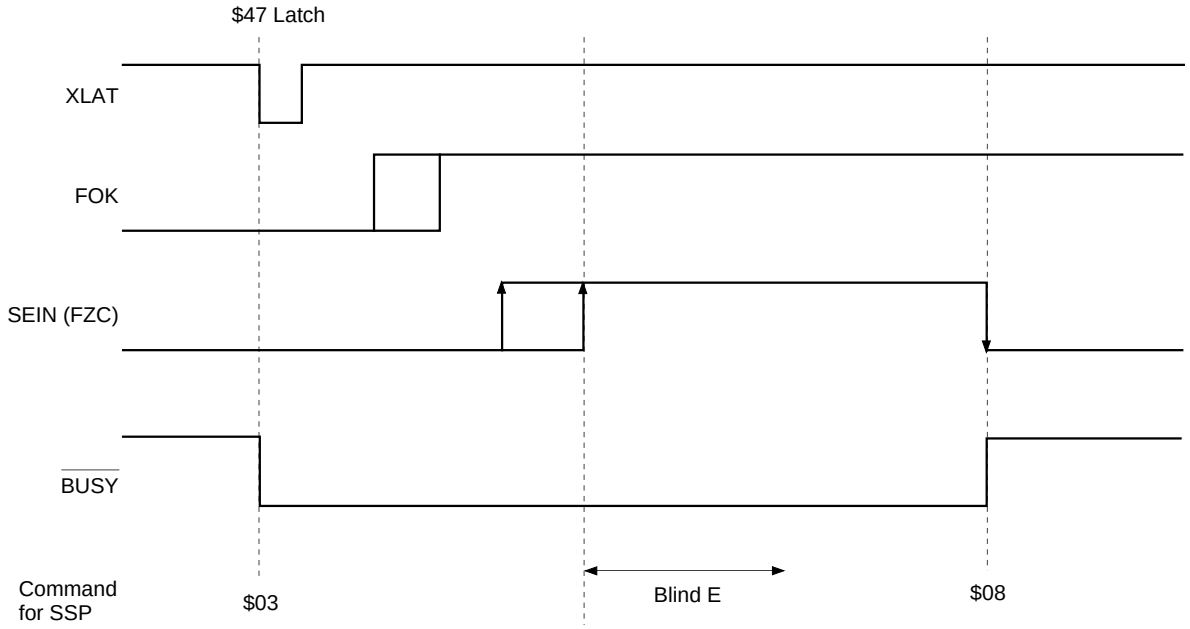


Fig. 2-18 (b). Auto Focus Timing Chart

(b) Track jump

1, 10 and 2N-track jumps are performed respectively. Always use them when focus, tracking, and sled servo are on. Note that tracking gain-up and braking-on ($17) should be sent beforehand because they are not performed.

- 1-track jump

  When $48 ($49 for REV) is received from the CPU, a FWD (REV) 1-track jump is performed in accordance with Fig. 2-19. Set blind A and brake B with register 5.

- 10-track jump

  When $4A ($4B for REV) is received from the CPU, a FWD (REV) 10-track jump is performed in accordance with Fig. 2-20. The principal difference between the 10-track jump and the 1-track jump is whether to kick the sled or not. In addition, after kicking the actuator, when 5 tracks have been counted through COUT, the brake is applied to the actuator. Then, when the actuator speed is found to have slowed up enough (determined by the COUT cycle becoming longer than the overflow C set in register 5), the tracking and sled servos are turned on.

- 2N-track jump

  When $4C ($4D for REV) is received from the CPU, a FWD (REV) 2N-track jump is performed in accordance with Fig. 2-21. The track jump count "N" is set in register 7. Although N can be set to 2^{16} tracks, note that the setting is actually limited by the actuator. COUT is used for counting the number of jumps when N is less than 16, and MIRR is used with N is 16 or higher.

  Although the 2N-track jump basically follows the same sequence as the 10-track jump, the one difference is that after the tracking servo is turned on, the sled continues to move only for "D", set in register 6.

- Fine search

  When $44 ($45 for REV) is received from the CPU, a FWD (REV) fine search (N-track jump) is performed in accordance with Fig. 2-22. The differences from a 2N-track jump are that a higher precision is achieved by controlling the traverse speed, and long jumps are possible by controlling the sled. The track jump count is set in register 7. N can be set to 2^{16} tracks. After kicking the actuator and sled, the traverse speed is controlled based on the overflow G. Set kick D and F in register 5. In addition, sled speed control during traverse can be turned off by causing COMP to fall. Set the number of tracks during which COMP falls in register B. After N tracks have been counted through COUT, the brake is applied to the actuator and sled. (This is performed by turning on the tracking servo for the actuator, and by kicking the sled in the opposite direction during the time for kick D set in register 6.) Then, the tracking and sled servos are turned on.

  Set overflow G to the speed required to slow up just before the track jump terminates. (The speed should be such that it will come on-track when the tracking servo turns on at the termination of the track jump.) For example, set the target track count N – α for the traverse monitor counter which is set in register B, and COMP will be monitored. When the falling edge of this COMP is detected, overflow G can be reset.

- M track move

  When $4E ($4F for REV) is received from the CPU, a FWD (REV) M track move is performed in accordance with Fig. 2-23. M can be set to 216 tracks. COUT is used for counting the number of moves when M is less than 16, and MIRR is used when M is 16 or higher. The M track move is executed only by moving the sled, and is therefore suited for moving across several thousand to several ten-thousand tracks. In addition, the track and sled servo are turned off after M tracks have been counted through COUT or MIRR unlike for the other jumps. Transfer $25 after the actuator is stabled.

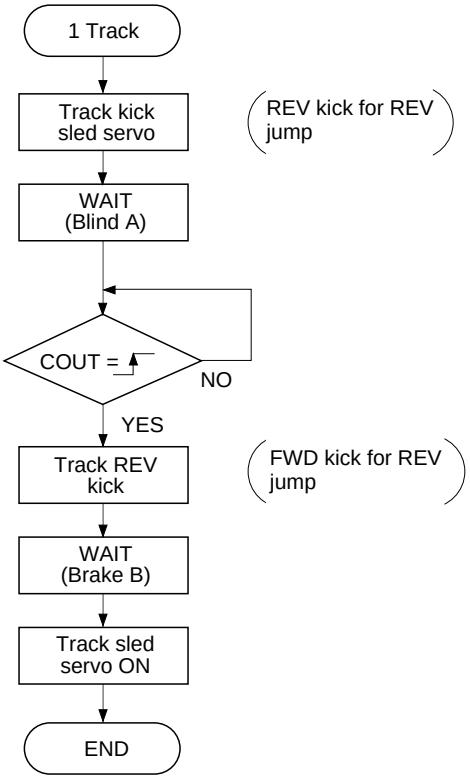


Fig. 2-19 (a). 1-Track Jump Flow Chart

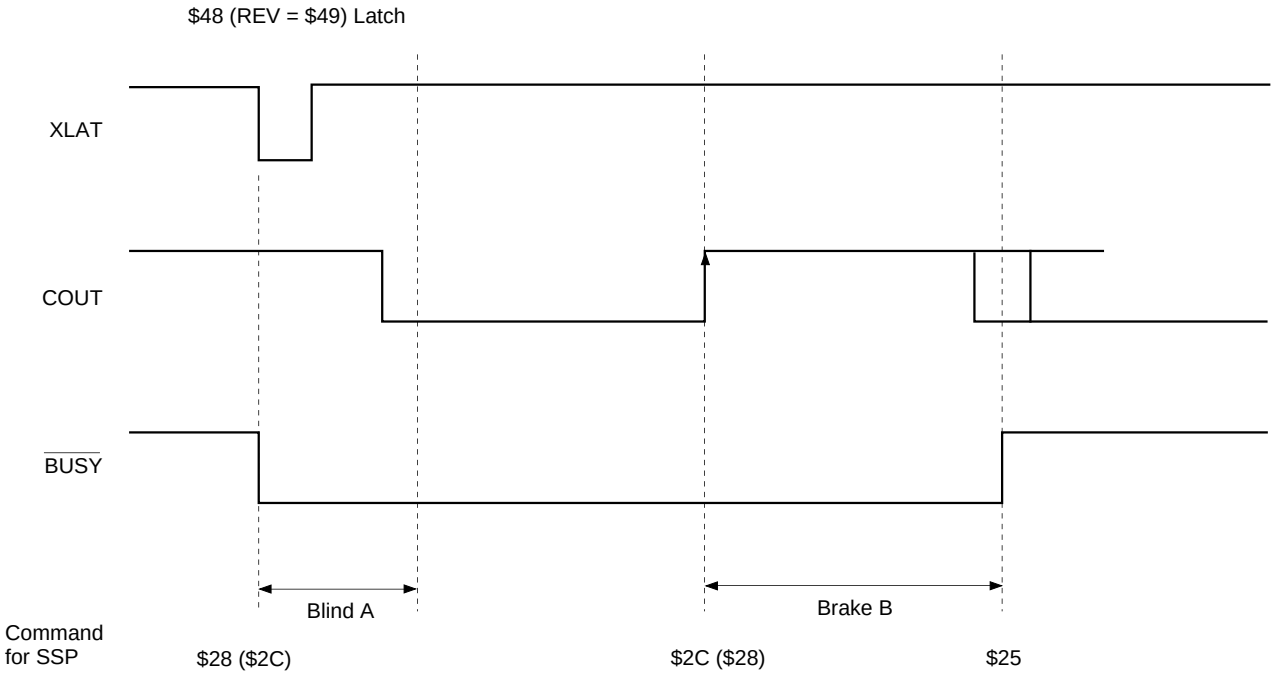


Fig. 2-19 (b). 1-Track Jump Timing Chart

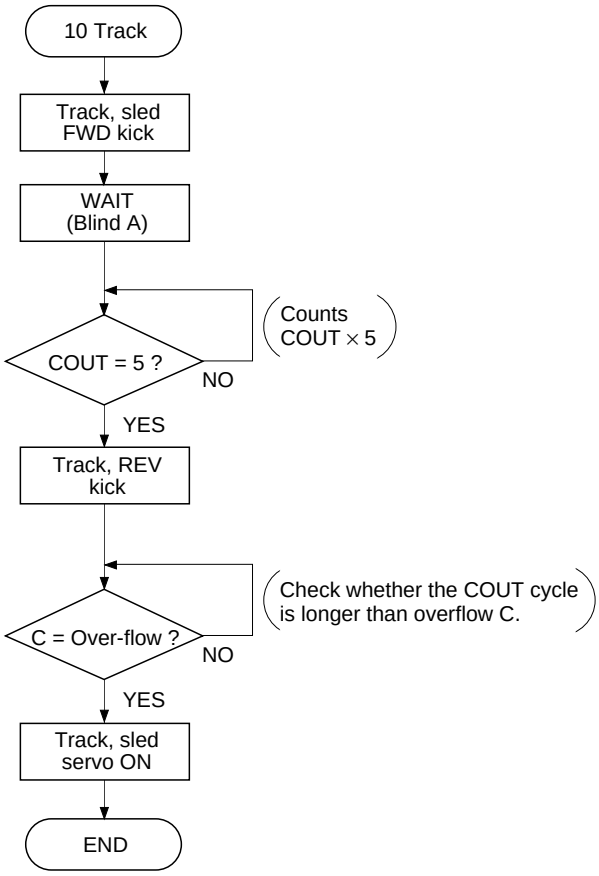


Fig. 2-20 (a). 10-Track Jump Flow Chart

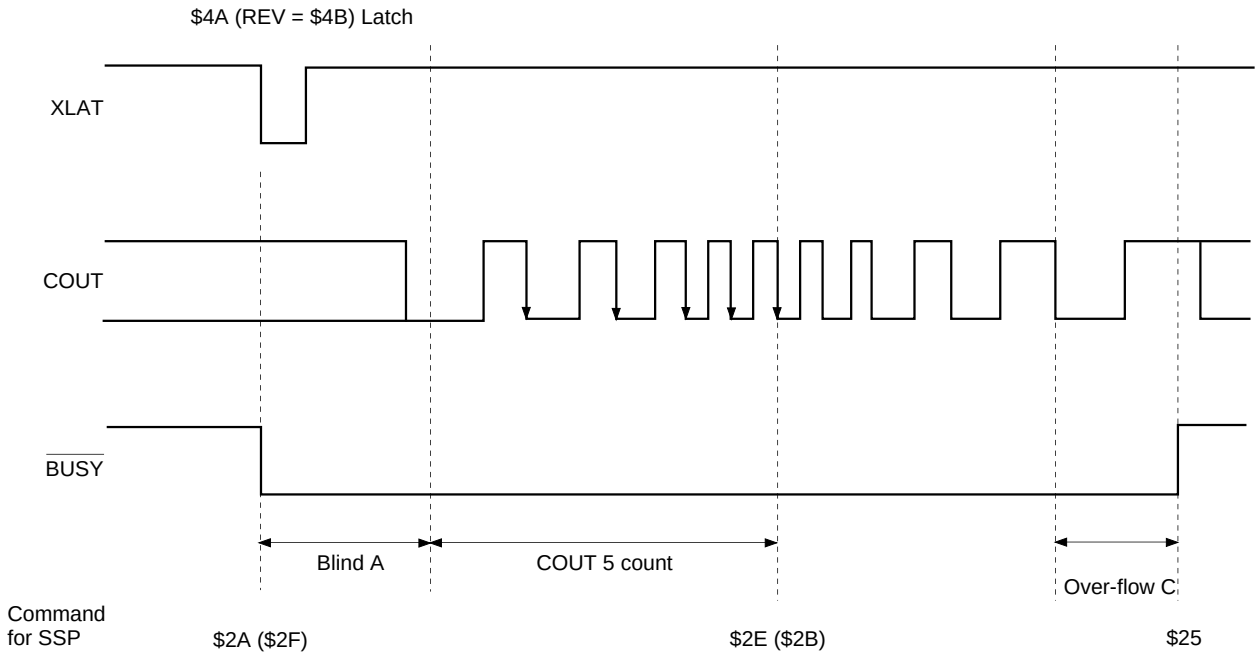


Fig. 2-20 (b). 10-Track Jump Timing Chart

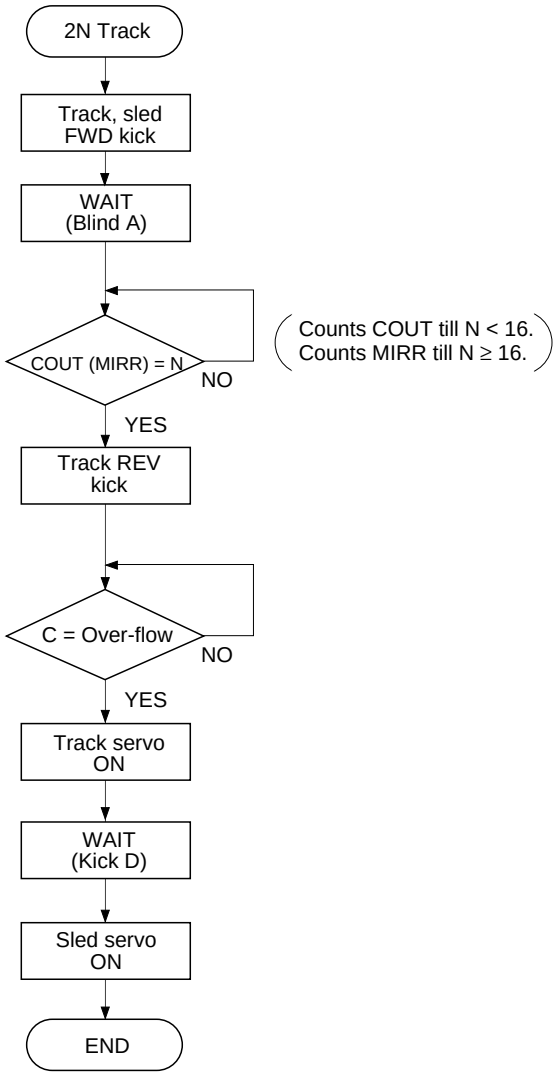


Fig. 2-21 (a). 2N-Track Jump Flow Chart

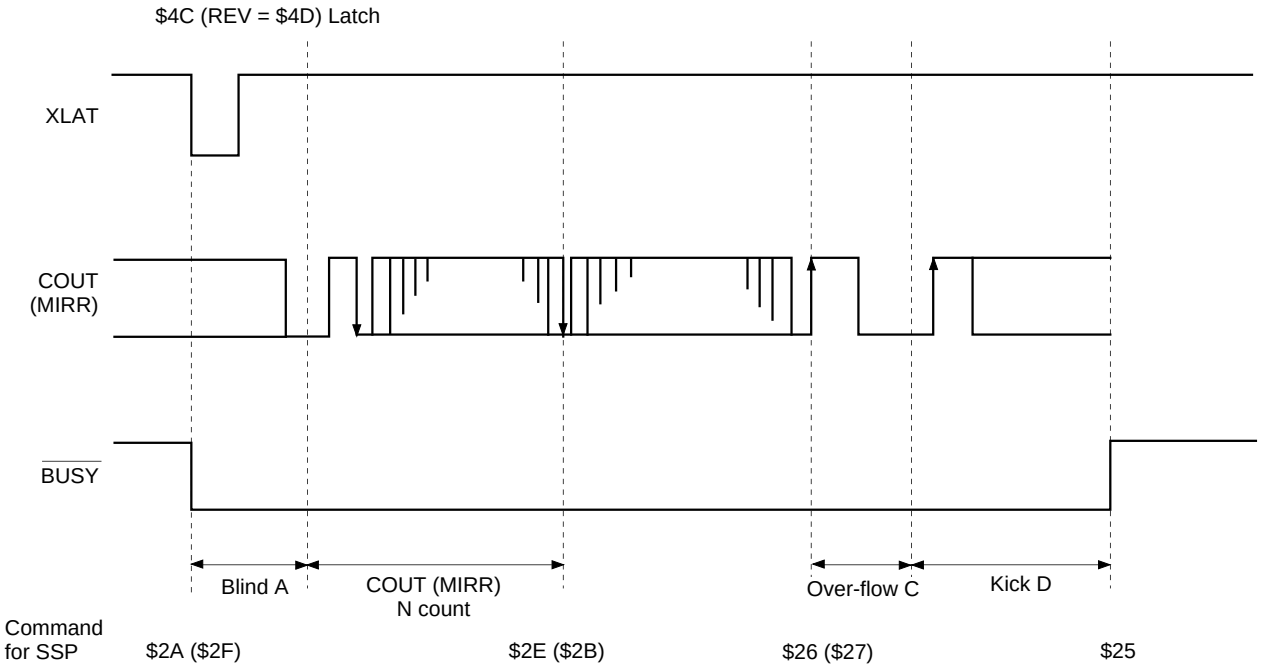


Fig. 2-21 (b). 2N-Track Jump Timing Chart

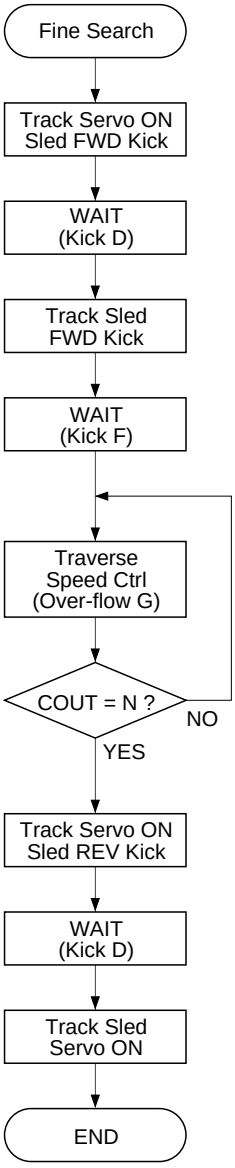


Fig. 2-22 (a). Fine Search Flow Chart

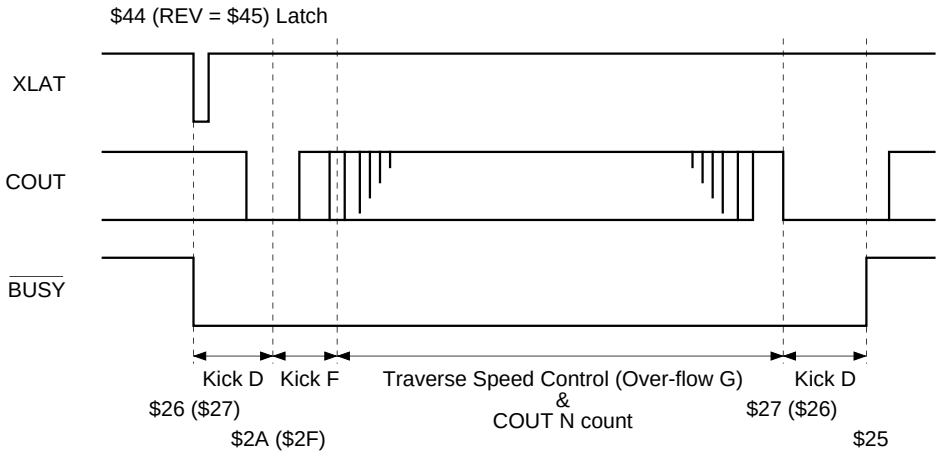


Fig. 2-22 (b). Fine Search Timing Chart

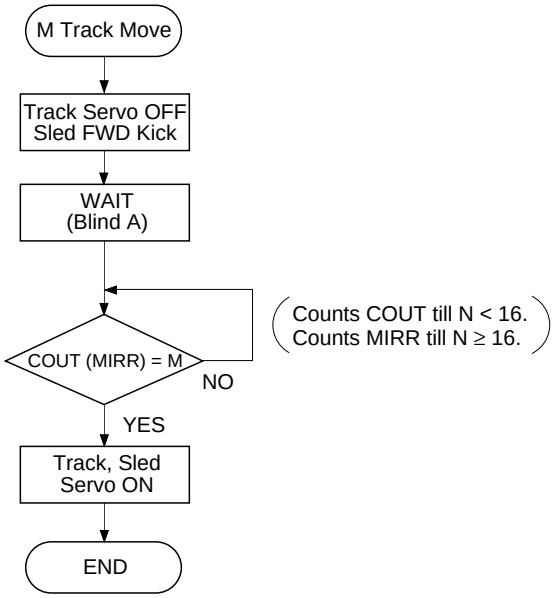


Fig. 2-23 (a). M-Track Move Flow Chart

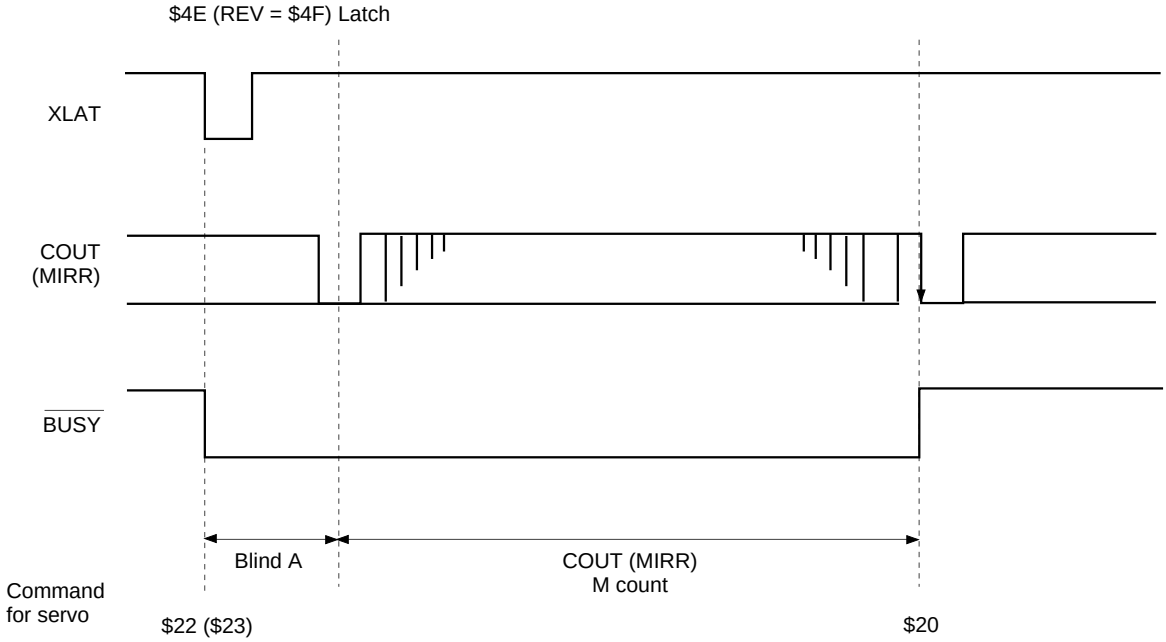
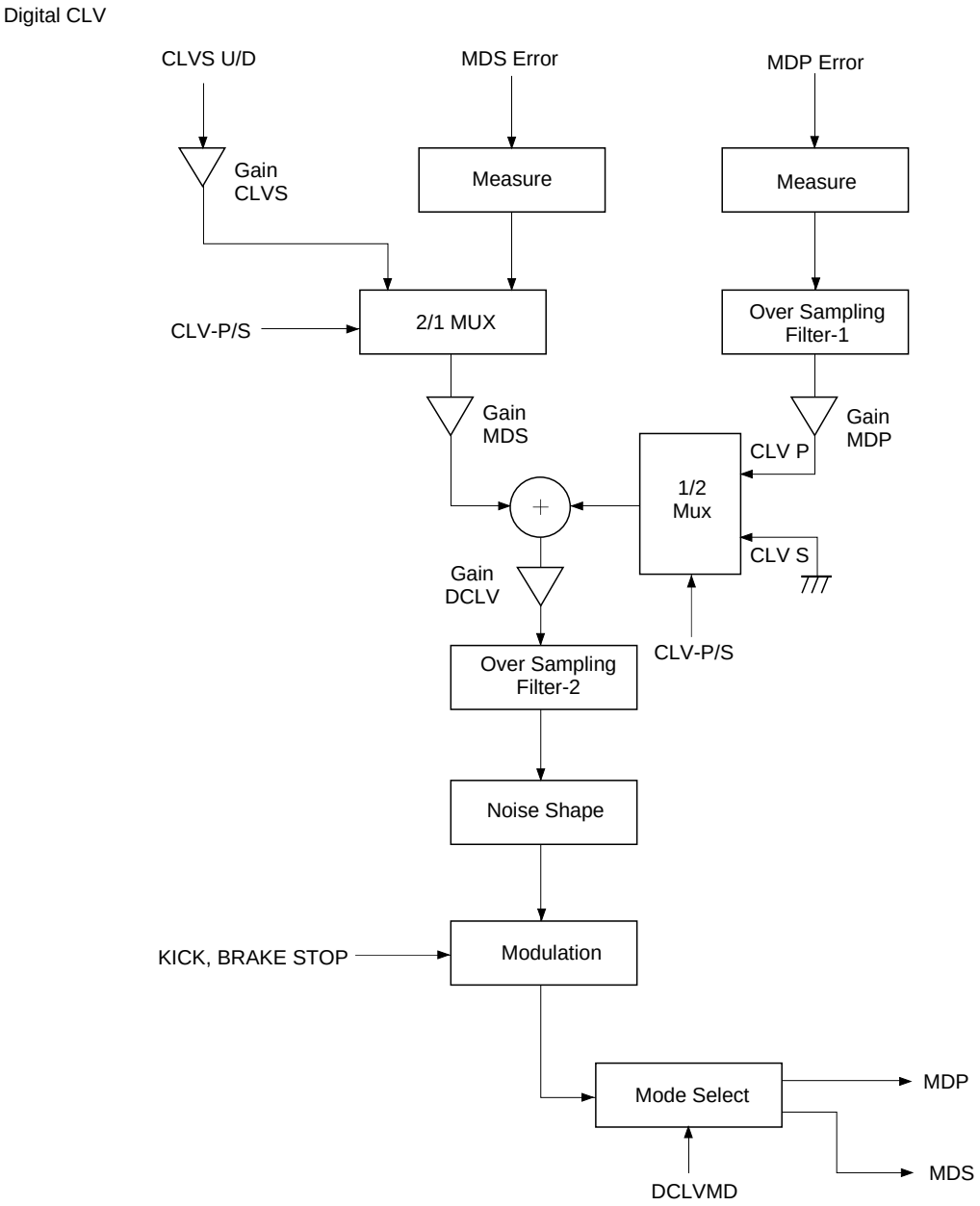


Fig. 2-23 (b). M-Track Move Timing Chart

§2-9. Digital CLV

Fig. 2-24 shows the block diagram. Digital CLV makes PWM output in CLVS, CLVP and other modes with the MDS error or MDP error signal sampling frequency increased to 130kHz during normal-speed operation.
In addition, the digital spindle servo can set the gain.



CLVS U/D: Up/down signal from the CLV-S servo
MDS error: Frequency error for the CLV-P servo
MDP error: Phase error for the CLV-P servo

Fig. 2-24. Block Diagram

§2-10. Asymmetry Compensation

Fig. 2-25 shows the block diagram and circuit example.

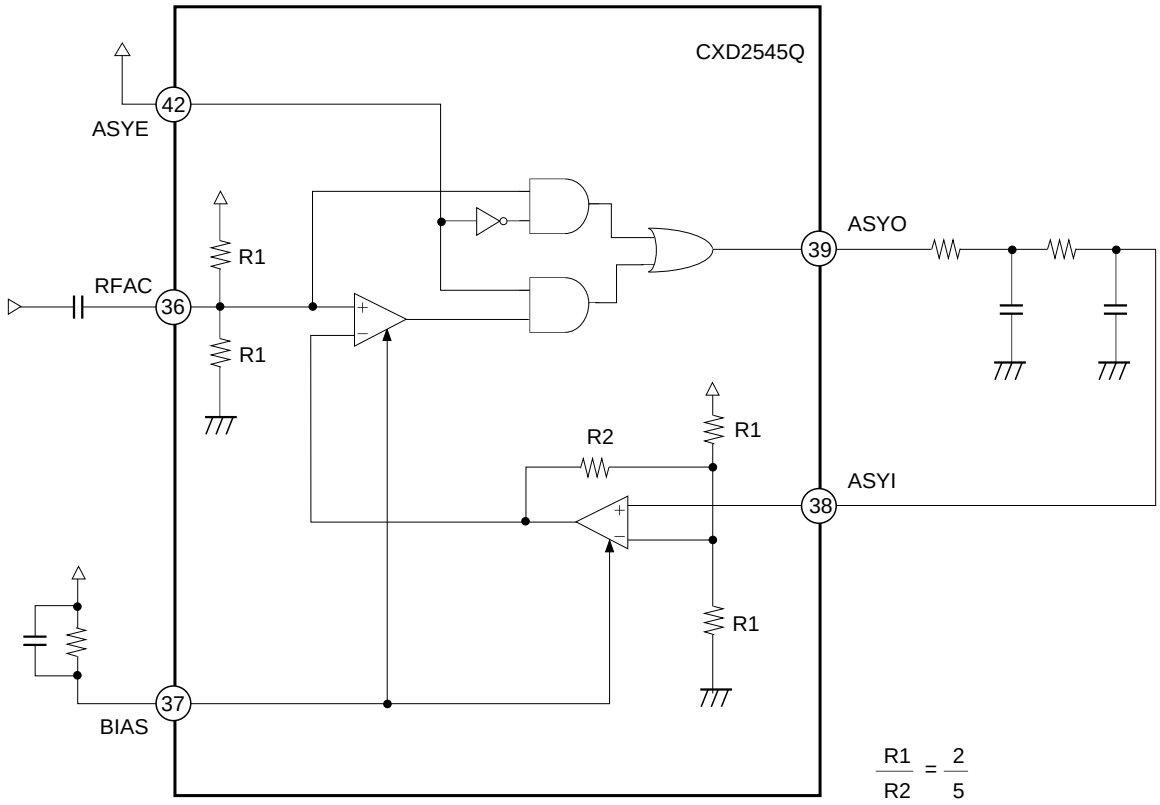


Fig. 2-25. Example of an Asymmetry Compensation Application Circuit

§2-11. Playback Speed

In the CXD2545Q, the following playback modes can be selected through different combinations of the crystal, XTSL pin, double-speed playback command (DSPB), VCO selection command (VCOSEL) and command transfer rate selector (ASHS). Also, the minimum operating voltage changes according to the playback mode. (See the Recommended Operating Conditions.)

Playback modes

Mode	X'tal	XTSL	DSPB	VCOSEL	ASHS	Playback speed	Error correction
1	768Fs	1	0	0/1	0	× 1	C1: double; C2: quadruple
2	768Fs	1	1	0/1	0	× 2	C1: double; C2: double
3	768Fs	0	0	1	1	× 2	C1: double; C2: quadruple
4	768Fs	0	1	1	1	× 4	C1: double; C2: double
5	384Fs	0	0	0/1	0	× 1	C1: double; C2: quadruple
6	384Fs	0	1	0/1	0	× 2	C1: double; C2: double
7	384Fs	1	1	0/1	0	× 1	C1: double; C2: double

However, Fs = 44.1kHz.

[3] Description of Servo Signal Processing-System Functions and Commands

§3-0. General Description of the Servo Signal Processing System (Voltages are the values for a 5V power supply.)

Focus servo

Sampling rate:	88.2kHz
Input range:	2.5V center ±1.0V
Output format:	7-bit PWM
Others:	Offset cancel
	Focus bias adjustment
	Focus search
	Gain-down function
	Defect countermeasure
	Automatic gain control

Tracking servo

Sampling rate:	88.2kHz
Input range:	2.5V center ±1.0V
Output format:	7-bit PWM
Others:	Offset cancel
	E:F balance adjustment
	Track jump
	Gain-up function
	Defect countermeasure
	Drive cancel
	Automatic gain control
	Vibration countermeasure

Sled servo

Sampling rate:	345Hz
Input range:	2.5V center ±1.0V
Output format:	7-bit PWM
Other:	Sled move

FOK, MIRR, DFCT signals generation

RF signal sampling rate:	1.4MHz
Input range:	2.15V to 5.0V
Others:	RF zero level automatic measurement
	The signal input from the RFDC pin is multiplied by a factor of 0.7 and loaded into the A/D converter.

§3-1. Digital Servo Block Master Clock (MCK)

The FSTI pin (Pin 66) is the reference clock input pin. The internal master clock (MCK) is generated by dividing the frequency of the signal input to FSTI. the frequency division ratio is 1/2 or 1/4.
Table 3-1 below shows the hypothetical case where the crystal clock generated from the digital signal processor block is 2/3 frequency divided and input to the FSTI pin (Pin 66) by externally connecting the FSTI pin (Pin 66) and the FSTO pin (Pin 67).
The XT4D and XT2D command settings can be made with D13 and D12 of $3F. (Default = 0)
The digital servo block is designed with an MCK frequency of 5.6448MHz.

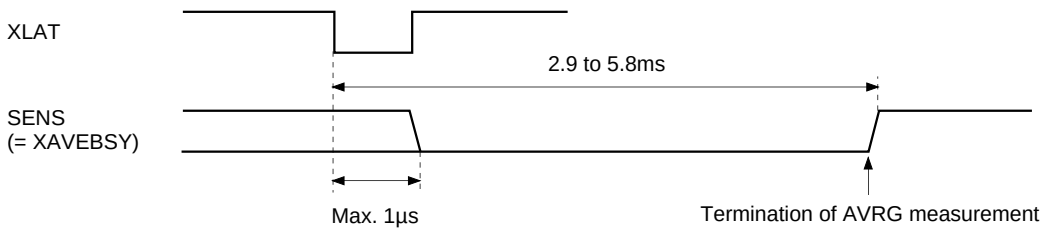
Mode	X'tal	FSTO	FSTI	XTSL	XT4D	XT2D	Frequency division ratio	MCK frequency
1	384Fs	256Fs	256Fs	*	0	1	1/2	128Fs
2	384Fs	256Fs	256Fs	0	0	0	1/2	128Fs
3	768Fs	512Fs	512Fs	*	1	0	1/4	128Fs
4	768Fs	512Fs	512Fs	1	0	0	1/4	128Fs

Fs = 44.1kHz, *: Don't care

Table 3-1.

§3-2. AVRG (Average) Measurement and Compensation

The CXD2545Q has a compensation circuit which performs compensation using the RFDC, VC, FE and TE AVRG measurement circuits and their measurement results in order to perform reliable servo control.
AVRG measurement and compensation is necessary to initialize the CXD2545Q, and can cancel the offset by performing each AVRG measurement before playback operation and using these results for compensation.
The level applied to the VC, FE, RFDC and TE pins can be measured by setting D15 (VLCM), D13 (FLM), D11 (RFLM) and D4 (TCLM) of $38 respectively to 1.
AVRG measurement consists of digitally measuring the level applied to each analog input pin by taking the average of 256 samples, and then loading these values into the AVRG register.
AVRG measurement requires approximately 2.9ms to 5.8ms after the command is received.
During AVRG measurement, if the upper 8 bits of the serial data are 38 (Hex), the termination of AVRG measurement operation can be confirmed by monitoring the SENS pin (Pin 80). (See the Timing Chart 3-2.)



Timing Chart 3-2.

<Measurement>

• VC AVRG

The offset can be canceled by measuring the VC level which is the center potential for the system and using that value to apply compensation to each input error signal.

• FE AVRG

This measures the FE signal DC level. In addition, compensation is applied to the FZC comparator level output from the SENS pin during FCS SEARCH (focus search) using these measurement results.

• TE AVRG

This measures the TE signal DC level.

• RF AVRG

The CXD2545Q generates the MIRR, DFCT and FOK signals from the RF signal. However, the FOK signal is generated by comparing the RF signal at a certain level, so that it is necessary to establish a zero level which becomes the comparator level reference. Therefore, the RF signal is measured before playback operation, and compensation applied to bring this level to the zero level.

An example of sending AVRG measurement and compensation commands is shown below.

(Example) $380800 (RF Avrg. measurement on)
$382000 (FE Avrg. measurement on)
$380010 (TE Avrg. measurement on)
$388000 (VC Avrg. measurement on)
(Finish each AVRG measurement before starting the next.)
$38140A (RFLC, FLC0, FLC1 and TLC1 commands on)
(The required compensation turn on together; see Fig. 3-3.)

An interval of 5.8ms or more must be maintained between each command, or the SENS pin must be monitored and the next AVRG command sent after confirming that the previous command has been finished.

<Compensation>

See Fig. 3-3 for the contents of each compensation below.

• RFLC

The difference by which the RF signal exceeds the RF AVRG value is input to the RF In register.
(00 is input when the RF signal is lower than the RF AVRG value.)

• TCL0

The value obtained by subtracting the VC AVRG value from the TE signal is input to the TRK In register.

• TCL1

The value obtained by subtracting the TE AVRG value from the TE signal is input to the TRK In register.

• VCLC

The value obtained by subtracting the VC AVRG value from the FE signal is input to the FCS In register.

• FLC1

The value obtained by subtracting the FE AVRG value from the FE signal is input to the FCS In register.

• FLC0

The value obtained by subtracting the FE AVRG value from the FE signal is input to the FZC register.

§3-3. E:F Balance Adjustment Function

When the disc is rotated with the laser on, and with the FCS (focus) servo on via FCS Search (focus search), the traverse waveform appears in the TE signal due to disc eccentricity.
In this condition, the low-band component can be extracted from the TE signal using the built-in TRK hold filter by setting D5 (TBLM) of $38 to 1.
The extracted low-band component is loaded into the TRVSC register as a digital value, and the TRVSC register value is established when TBLM returns to 0.
Next, setting D2 (TLC2) of $38 to 1 applies only the amount of compensation (subtraction) equal to the TRVSC register value to the values obtained from the TE and SE input pins, enabling the E:F balance offset to be adjusted. (See Fig. 3-3.)

§3-4. FCS Bias (Focus Bias) Adjustment Function

The FBIAS register value can be added to the FCS servo filter input by setting D14 (FBON) of $3A to 1. (See Fig. 3-3.)
When the FBIAS register value is set to D11 = 0 and D10 = 1 by $34F, data can be written using the 9-bit value of D9 to D1 (D9: MSB).
In addition, the RF jitter can be monitored by setting the SOCT command of $8 to 1. (See the CD Signal Processing-System Block Timing Chart 2-4.)

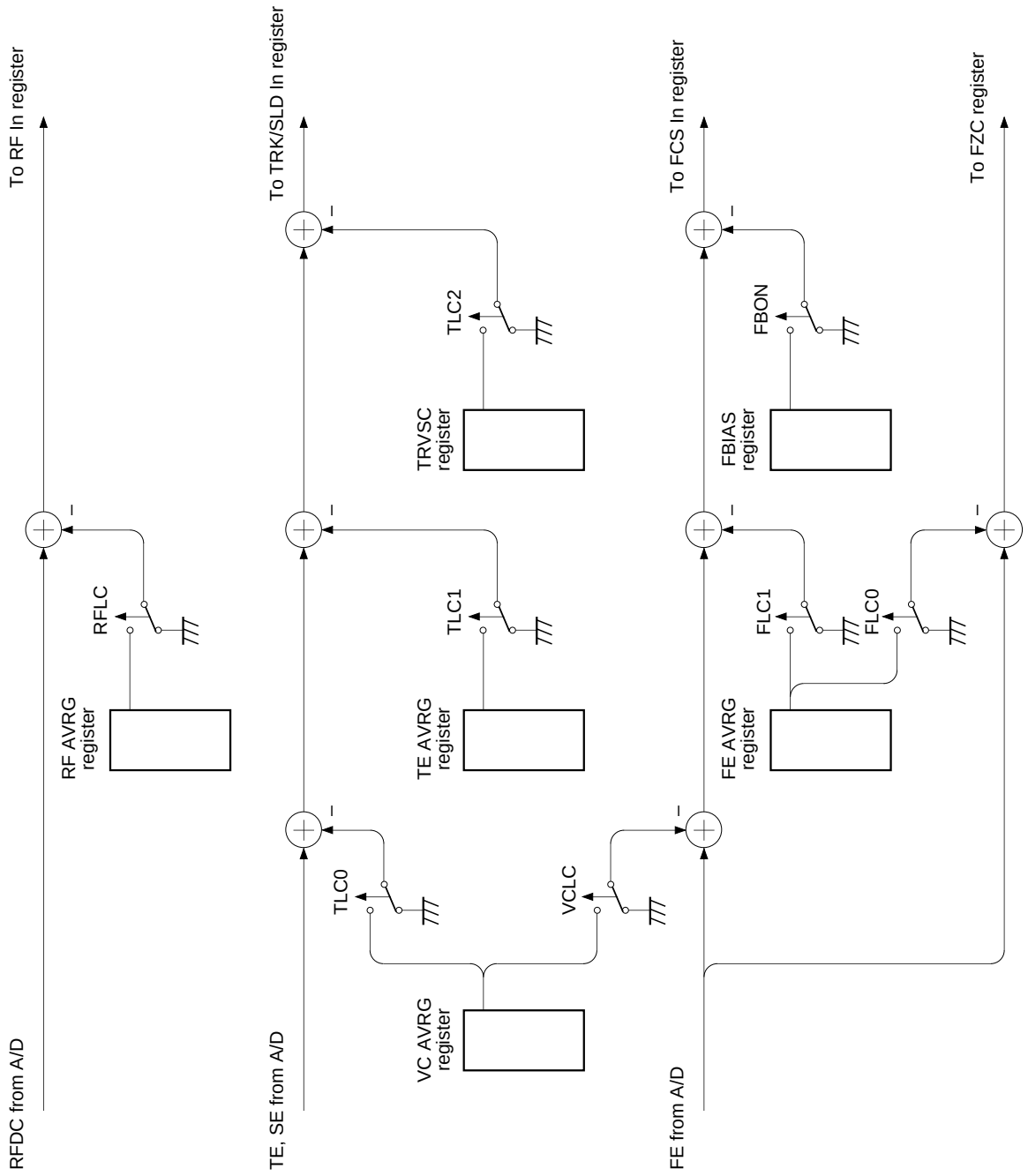
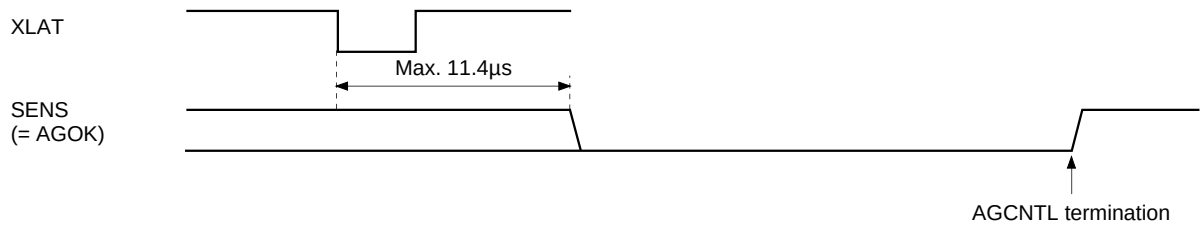

To RF In register
To TRK/SLD In register
To FCS In register
To FZC register
RFDC from A/D
TE, SE from A/D
FE from A/D
RF AVRG register
RFLC
TE AVRG register
TLC1
TRVSC register
TLC2
VC AVRG register
TLC0
VCLC
FE AVRG register
FLC1
FLC0
FBIAS register
FBON

Fig. 3-3.

§3-5. AGCNTL (Automatic Gain Control) Function

The AGCNTL function automatically adjusts the filter internal gain in order to obtain the appropriate gain with the servo loop. AGCNTL not only copes with the sensitivity variation of the actuator and photo diode, etc., but also obtains the optimal gain for each disc.
The AGCNTL command is sent when each servo is turned on. During AGCNTL operation, if the upper 8 bits of the input serial data are 38 (Hex), the termination of AGCNTL operation can be confirmed by monitoring the SENS pin (Pin 80). (See the Timing Chart 3-4 and the Description of SENS Signals.)
Setting D9 and D8 of $38 to 1 set FCS (focus) and TRK (tracking) respectively to AGCNTL operation.

Note) When performing AGCNTL operation, each servo filter must be in the gain normal status, and the anti-shock circuit (described hereafter) must be disabled.



Timing Chart 3-4.

Coefficient K13 changes for AGF (focus AGCNTL) and coefficients K23 and K07 for AGT (tracking AGCNTL) due to AGCNTL.
These coefficients change from 01 to 7F (Hex), and they must also be set within this range when written externally.
After AGCNTL operation has terminated, these coefficient values can be confirmed by reading them out from the SENS pin with the serial readout function (described hereafter).

AGCNTL related settings

The following settings can be changed with $35, $36 and $37.

FG6 to FG0; AGF convergence gain setting, effective setting range: 00 to 57 (Hex)
TG6 to TG0; AGT convergence gain setting, effective setting range: 00 to 57 (Hex)
AGS; Self-stop on/off
AGJ; Convergence completion judgment time
AGGF; Internally generated sine wave amplitude (AGF)
AGGT; Internally generated sine wave amplitude (AGT)
AGV1; AGCNTL sensitivity 1 (during high sensitivity adjustment)
AGV2; AGCNTL sensitivity 2 (during low sensitivity adjustment)
AGHS; High sensitivity adjustment on/off
AGHT; High sensitivity adjustment time

Note) Converging servo loop gain values can be changed with the FG6 to 0 and TG6 to 0 setting values. In addition, these setting values must be within the effective setting range. The default settings aim for 0dB at 1kHz. However, since convergence values vary according to the characteristics of each constituent element of the servo loop, FG and TG values should be set as necessary.

AGCNTL and default operation have two stages.
In the first stage, high sensitivity adjustment is performed for a certain period of time (select 256/128ms with AGHT), and the AGCNTL coefficient approaches the appropriate value. The sensitivity at this time can be selected from two types with AGV1.
In the second stage, the AGCNTL coefficient is led reliably towards the appropriate value at a relatively low sensitivity. The sensitivity for the second stage can be selected from two types with AGV2. In the second stage of default operation, when the AGCNTL coefficient reaches the appropriate value and stops changing, the CXD2545Q confirms that the AGCNTL coefficient has not changed for a certain period of time (select 63/31ms with AGHJ), and then terminates AGCNTL operation. (Self-stop mode)
This self-stop mode can be canceled by rewriting AGS to 0.
In addition, the first stage is omitted for AGCNTL operation when AGHS is set to 0.
An example of AGCNTL coefficient transitions during AGCNTL operation and the relationship between the various settings are shown in Fig. 3-5.

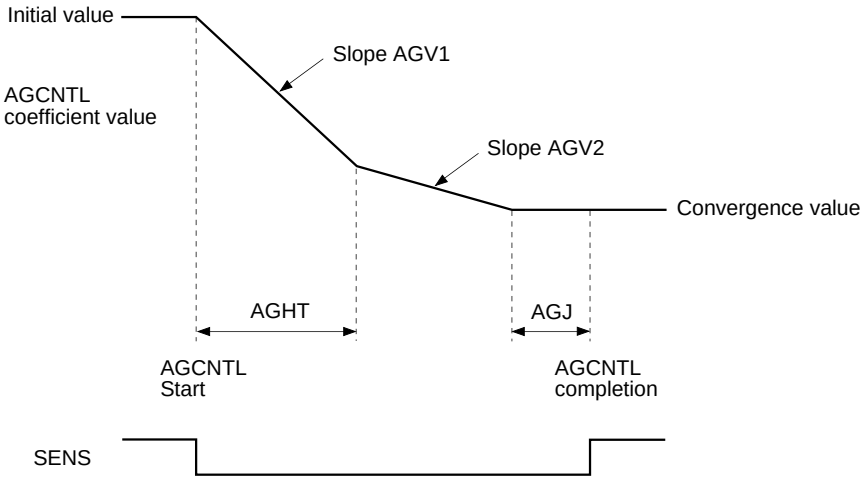


Fig. 3-5.

§3-6. FCS Servo and FCS Search (Focus Search)

The FCS servo is controlled by the 8-bit serial command $0X. (See Table 3-6.)

Register name	Command	D23 to D20	D19 to D16	
0	FOCUS CONTROL	0 0 0 0	1 0 ∗ ∗	FOCUS SERVO ON (FOCUS GAIN NORMAL)
			1 1 ∗ ∗	FOCUS SERVO ON (FOCUS GAIN DOWN)
			0 ∗ 0 ∗	FOCUS SERVO OFF, 0V OUT
			0 ∗ 1 ∗	FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT
			0 ∗ 1 0	FOCUS SEARCH VOLTAGE DOWN
			0 ∗ 1 1	FOCUS SEARCH VOLTAGE UP

∗: Don't care

Table 3-6.

FCS Search

FCS search is required in the course of turning on the FCS servo.

Figs. 3-7 and 3-8 show the signals for sending commands $00 → $02 → $03 and performing only FCS search operation, and for moving from $03 to FCS on ($08).

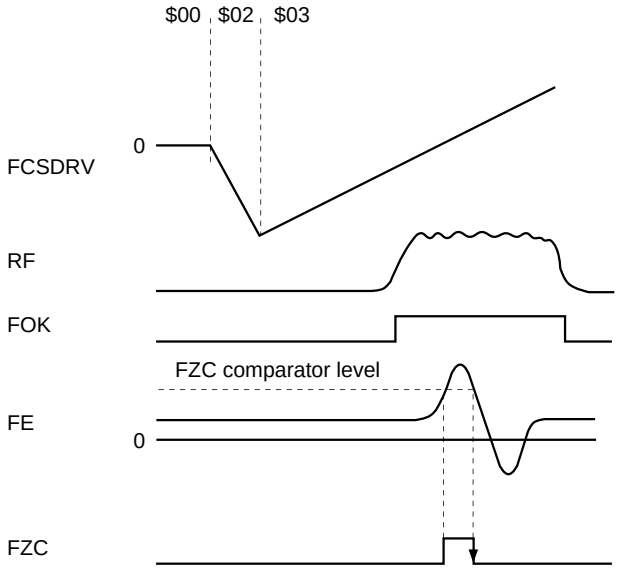


Fig. 3-7.

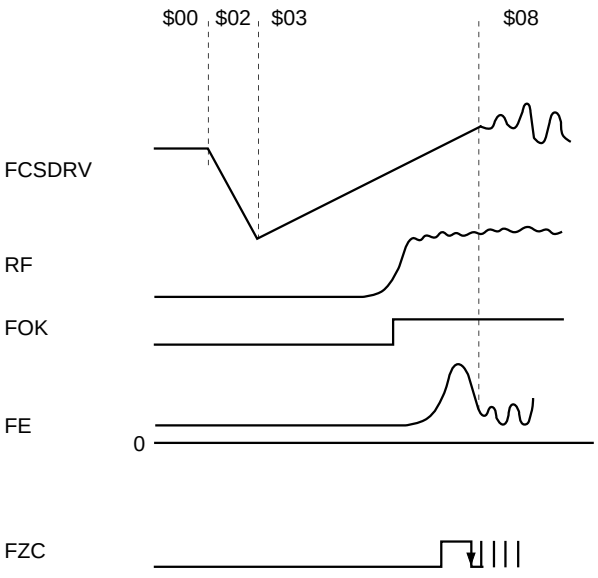


Fig. 3-8.

§3-7. TRK (Tracking) and SLD (Sled) Servo Control

TRK and SLD servo control is performed by the 8-bit command $2X. (See Table 3-9.)
When the upper 4 bits of the serial data are 2 (Hex), TZC is output to the SENS pin.

Register name	Command	D23 to D20	D19 to D16	
2	TRACKING MODE	0 0 1 0	0 0 ∗ ∗	TRACKING SERVO OFF
			0 1 ∗ ∗	TRACKING SERVO ON
			1 0 ∗ ∗	FORWARD TRACK JUMP
			1 1 ∗ ∗	REVERSE TRACK JUMP
			∗ ∗ 0 0	SLED SERVO OFF
			∗ ∗ 0 1	SLED SERVO ON
			∗ ∗ 1 0	FORWARD SLED MOVE
			∗ ∗ 1 1	REVERSE SLED MOVE

∗: Don't care

Table 3-9.

TRK Servo

The TRK JUMP (track jump) height can be set with the 6 bits D13 to D8 of $36.
In addition, when the TRK servo is on, the TRK servo filter assumes gain-up status when D17 of $1 is set to 1. The TRK servo filter also assumes gain-up status when vibration detection is performed with the LOCK signal (Pin 98) low and the anti-shock circuit (described hereafter) enabled.
The gain-up filter used when TRK has assumed gain up status has two types of structures which can be selected by setting D16 of $1. (See Table 3-17.)

SLD Servo

The SLD MOV (sled move) output, composed of a basic value from the 6 bits D13 to D8 of $37, is determined by multiplying this value by the × 1, × 2, × 3 or × 4 magnification set using D17 and D16 when D19 = D18 = 0 is set with $3. (See Table 3-10.)
SLD MOV must be performed continuously for 50µs or more. In addition, if the LOCK input signal goes low when the SLD servo is on, the SLD servo turns off.

Note) When the LOCK signal is low, the operations which set the TRK servo to gain up status and turn off the SLD servo can be canceled by setting D6 (LKSW) of $38 to 1.

Register name	Command	D23 to D20	D19 to D16	
3	SELECT	0 0 1 1	0 0 0 0	SLED KICK LEVEL (basic value × ±1)
			0 0 0 1	SLED KICK LEVEL (basic value × ±2)
			0 0 1 0	SLED KICK LEVEL (basic value × ±3)
			0 0 1 1	SLED KICK LEVEL (basic value × ±4)

Table 3-10.

§3-8. MIRR and DFCT Signal Generation

The RF signal obtained from the RFDC pin (Pin 26) is sampled at approximately 1.4MHz and loaded.
The MIRR and DFCT signals are generated from this RF signal.

MIRR Signal Generation

The loaded RF signal is applied to peak hold and bottom hold circuits.
An envelope is generated from the waveforms generated in these circuits, and the MIRR comparator level is generated from the average of these envelope waveforms.
The MIRR signal is generated by comparing this MIRR comparator level with the waveform generated by subtracting the bottom hold value from the peak hold value. (See Fig. 3-11.)

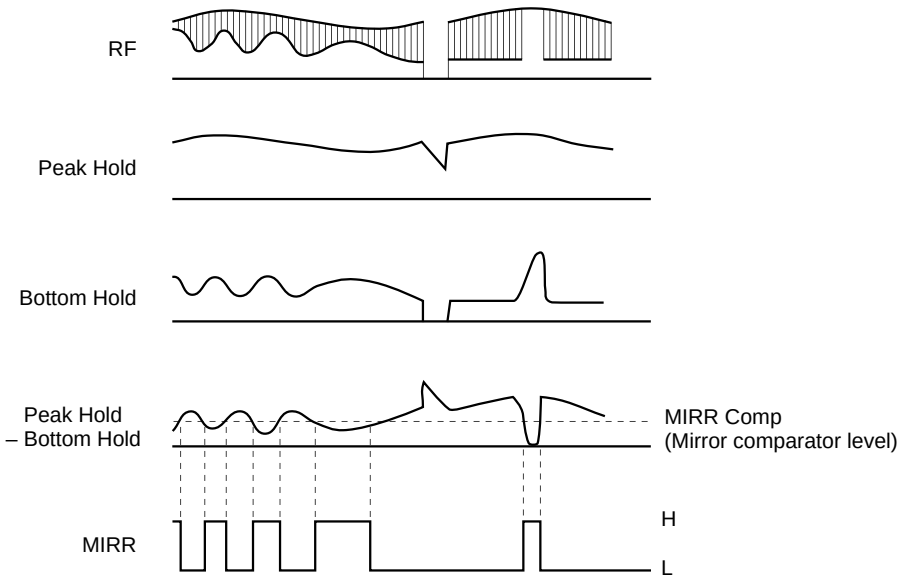


Fig. 3-11.

DFCT Signal Generation

The loaded RF signal is input to two peak hold circuits with different time constants, and the DFCT signal is generated by comparing the difference between these two peak hold waveforms with the DFCT comparator level. (See Fig. 3-12.)
The DFCT comparator level can be selected from four values using D13 and D12 of $3B.

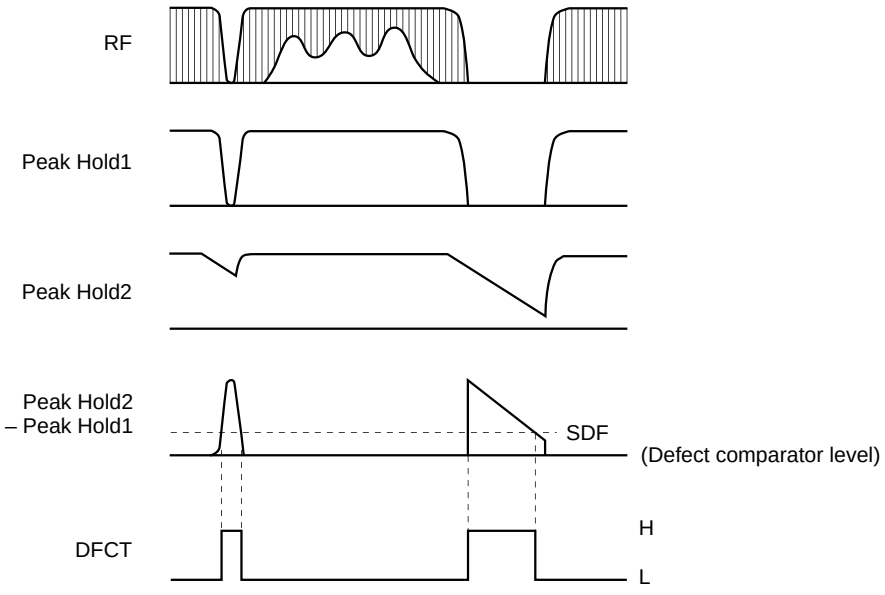


Fig. 3-12.

§3-9. DFCT Countermeasure Circuit

The DFCT countermeasure circuit performs operations to maintain the directionality of the servo so that the servo does not become easily dislocated due to scratches or defects on discs.
Specifically, these operations are achieved by performing scratch and defect detection with the DFCT signal generation circuit, and when DFCT goes high, applying the low frequency element of the error signal before DFCT went high to the FCS and TRK servo filter inputs.
In addition, these operations are activated by the default. They can be disabled by setting D7 (DFSW) of $38 to 1 or by inputting high level to the DFSW pin (Pin 84).

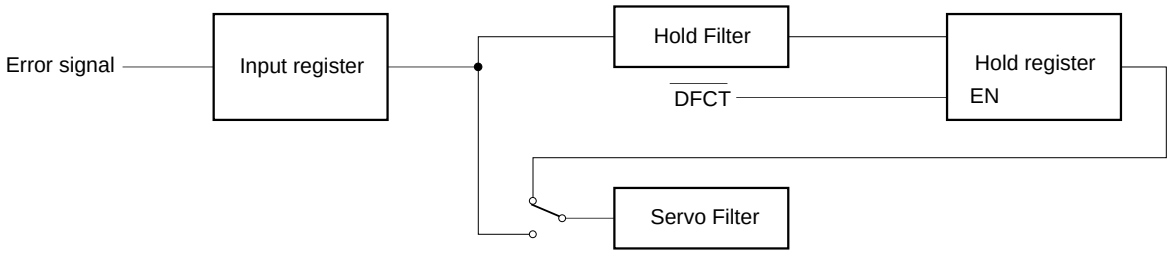


Fig. 3-13.

§3-10. Anti-Shock Circuit

When vibrations are produced in the CD player, this circuit forces the TRK filter to assume gain-up status so that the servo does not become easily dislocated. This circuit should be considered for systems which require vibration countermeasures.
Specifically, vibrations are detected using an internal anti-shock filter and comparator circuit, and the gain is increased. (See Fig. 3-14.)
The comparator level is fixed to 1/16 of the maximum comparator input amplitude. However, the comparator level can essentially be adjusted by adjusting the value of the anti-shock filter output coefficient K35.
This function can be turned on and off by D19 of $1 when the brake circuit (described hereafter) is off. (See Table 3-17.)
This circuit can also support an external vibration detection circuit, and can also set the TRK servo filter to gain up status by inputting high level to the ATSK pin (Pin 85).
When the serial data is $1, vibration detection can be monitored from the SENS pin.

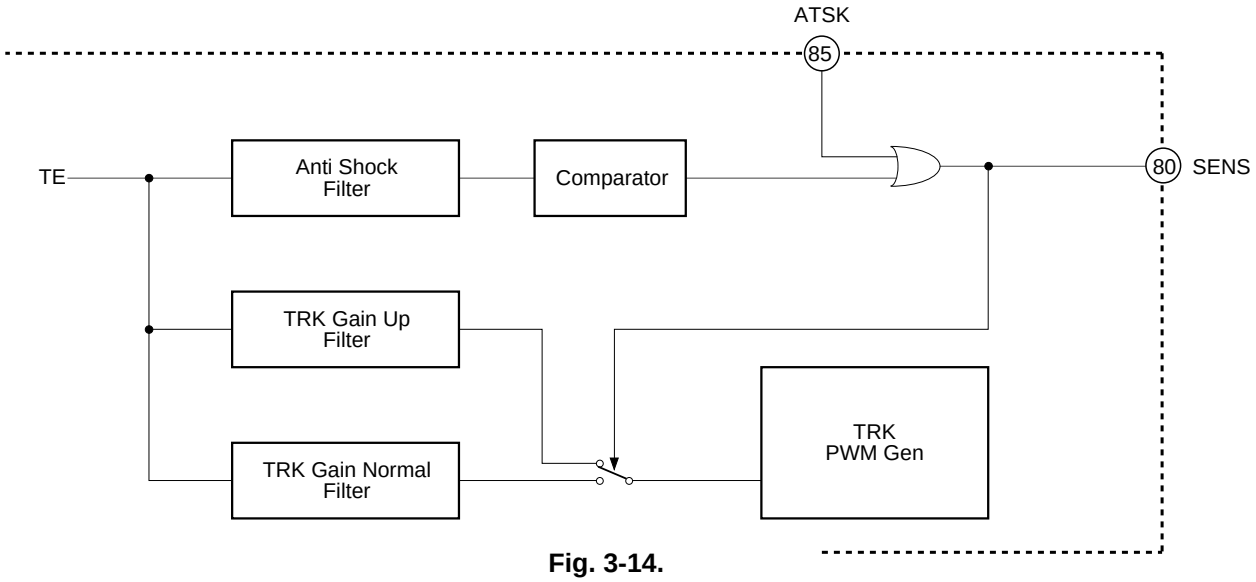


Fig. 3-14.

§3-11. Brake Circuit

Immediately after a track jump of a certain size or more, the actuator setting worsens and it becomes difficult to return the servo suddenly to the on status.
The brake circuit prevents these types of phenomenon from occurring.
In principle, this circuit cuts unnecessary portions of the tracking drive and applies the brake by utilizing the 180° offset in the RF envelope and tracking error phase relationship which occurs when the actuator cuts across the track in the radial direction from the inner track to the outer track and vice versa. (See Figs. 3-15 and 3-16.)
Specifically, this operation is achieved by masking the tracking drive using the TRKCNCL signal generated by loading the MIRR signal at the edge of the TZC (Tracking Zero Cross) signal.
The brake circuit can be turned on and off by D18 of $1. (See Fig. 3-17.)

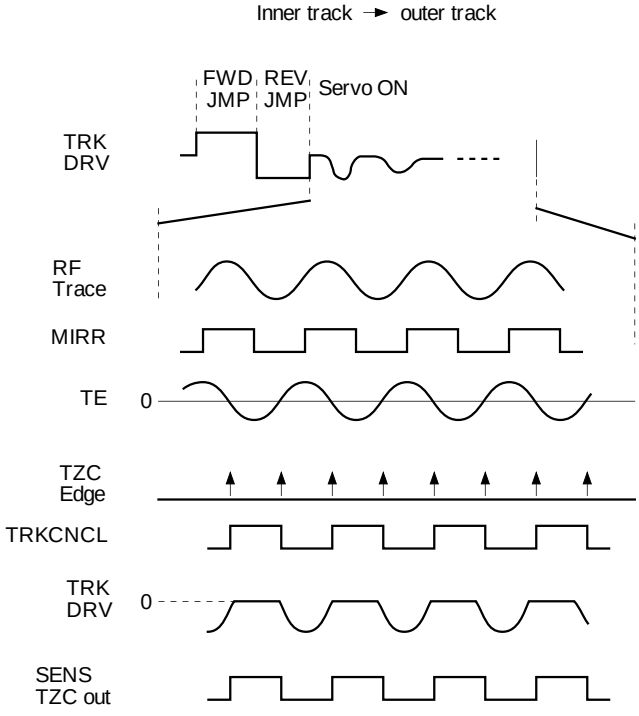


Fig. 3-15.

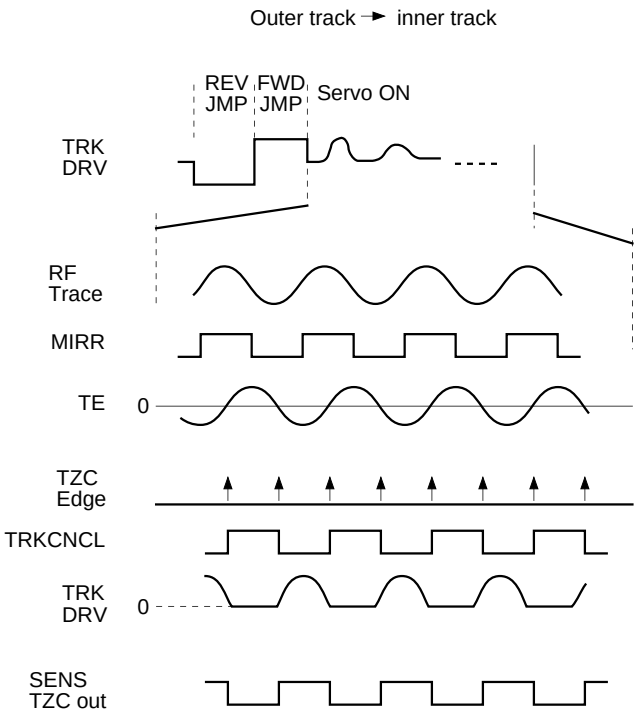


Fig. 3-16.

Register name	Command	D23 to D20	D19 to D16	
1	TRACKING CONTROL	0 0 0 1	1 0 * *	ANTI SHOCK ON
			0 * * *	ANTI SHOCK OFF
			* 1 * *	BRAKE ON
			* 0 * *	BRAKE OFF
			* * 0 *	TRACKING GAIN NORMAL
			* * 1 *	TRACKING GAIN UP
			* * * 1	TRACKING GAIN UP FILTER SELECT 1
			* * * 0	TRACKING GAIN UP FILTER SELECT 2

*: Don't care

Fig. 3-17.

§3-12. COUT Signal

The COUT signal is output in order to count the number of tracks passed over during traverse, etc. It is basically generated by loading the MIRR signal at both edges of the TZC signal. However, the used TZC signal can be selected and there are two types of output methods according to the COUT signal application.

1-track jumps, etc.
Fast phase COUT signal generation is performed using a fast phase TZC signal.

High-speed traverse
During high-speed traverse, reliable COUT signal generation is performed using a delayed phase TZC signal.

This is because some time is required to generate the MIRR signal, and it is necessary to delay the TZC signal in accordance with the MIRR signal delay during high-speed traverse.
The COUT signal output method is switched with D16 when D19 = D18 = 1 and D17 = 0 are set with $3. (when D16 = 1, for delayed phase and high-speed traverse). In addition, the TZC signal delay can be selected from two values with D14 of $36.

§3-13. Serial Readout Circuit

The following measurement and adjustment results which have been specified in advance can be read out from the SENS pin (Pin 80) by inputting the readout clock to the SCLK pin (Pin 83) using serial command $39. (See Fig. 3-18, Table 3-19 and the Description of SENS Signals.)

Specified commands
$390C: VC AVRG measurement result
$3908: FE AVRG measurement result
$3904: TE AVRG measurement result
$391F: RF AVRG measurement result
$3953: FCS AGCNTL coefficient result
$3963: TRK AGCNTL coefficient result
$391C: TRVSC adjustment result
$391D: FBIAS register value

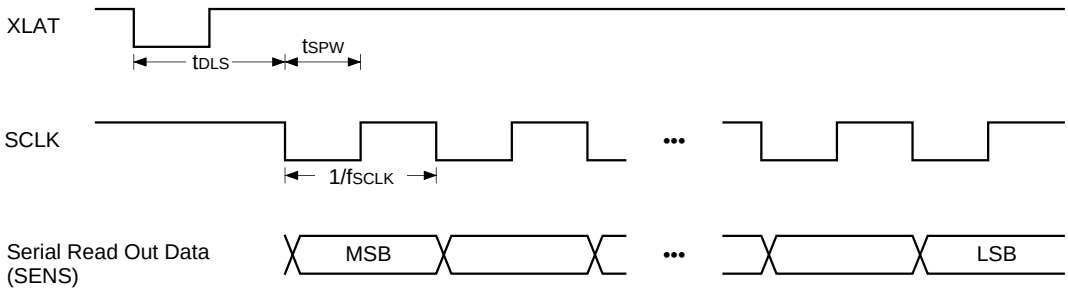


Fig. 3-18.

Item	Symbol	Min.	Typ.	Max.	Unit
SCLK frequency	f_{SCLK}			1	MHz
SCLK pulse width	t_{SPW}	500			ns
Delay time	t_{DLS}	15			µs

Table 3-19.

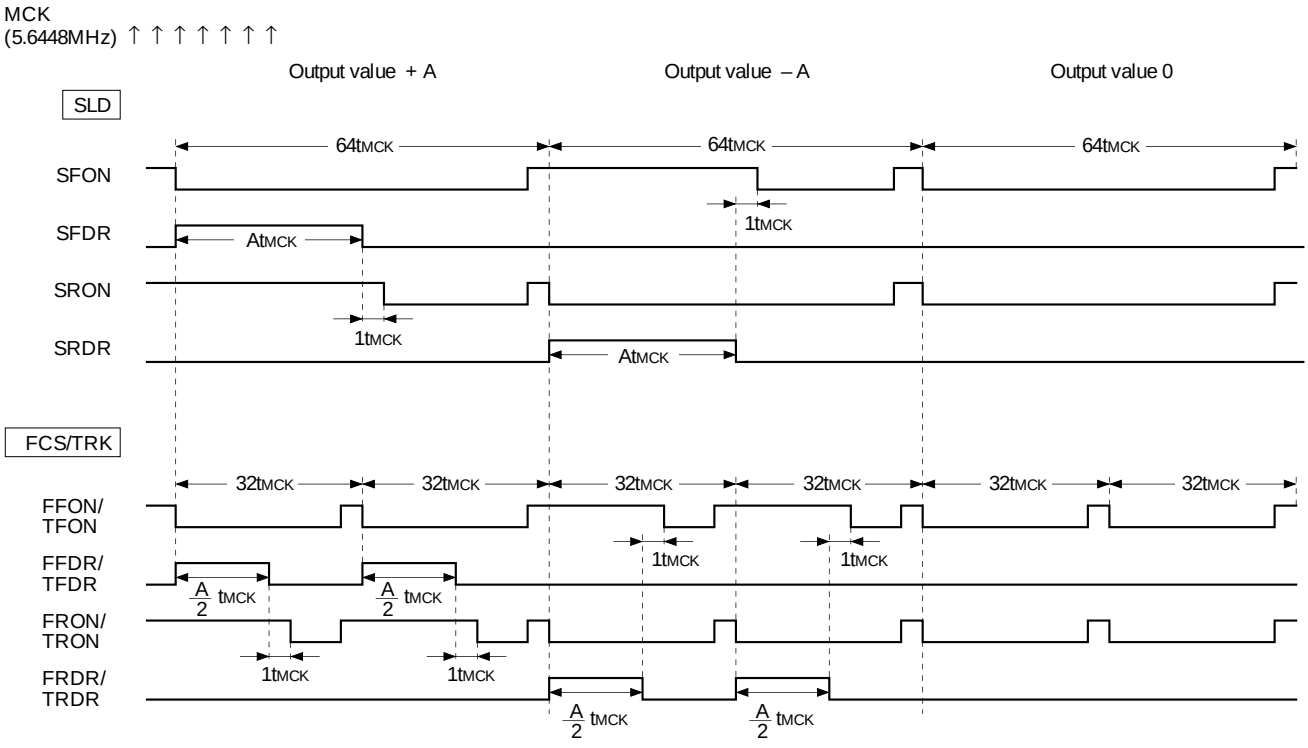
During readout, the upper 8 bits of the serial data must be 39 (Hex).

§3-14. Writing the Coefficient RAM

The coefficient RAM can be rewritten by $34. All coefficients have default values in the built-in ROM, and transfer from the ROM to the RAM is completed approximately 40µs after the XRST pin (Pin 81) rises. (The coefficient RAM cannot be rewritten during this period.)
After that, the characteristics of each built-in filter can be finely adjusted by rewriting the data for each address of the coefficient RAM.
The coefficient rewrite command is comprised of 24 bits, with D14 to D8 of $34 as the address (D15 = 0) and D7 to D0 as data.

§3-15. PWM Output

FCS, TRK and SLD outputs are output as PWM waveforms.
In particular, FCS and TRK permit accurate drive by using a double oversampling noise shaper.
Timing Chart 3-20 and Figs. 3-21 and 3-22 show examples of output waveforms and drive circuits.



The ON signal (FON and RON) is active low.

$$t_{MCK} = \frac{1}{5.6448MHz} \approx 180ns$$

Timing Chart 3-20.

Example of Driver Circuits

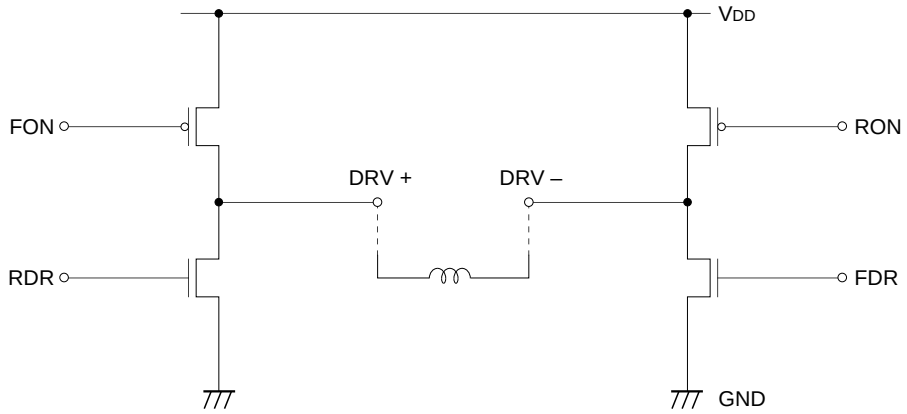


Fig. 3-21. PWM Bridge Drive Circuit

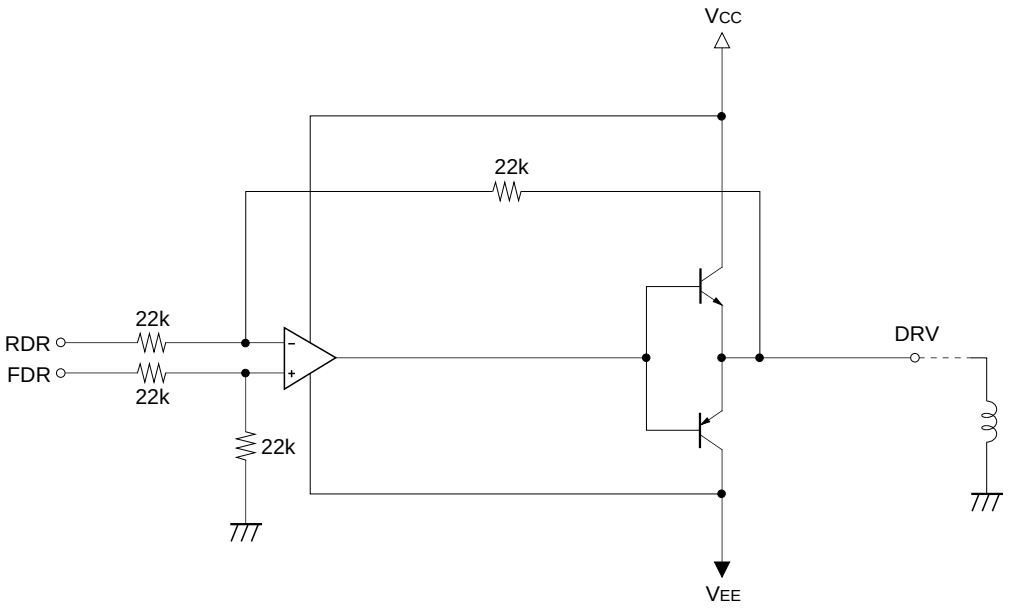
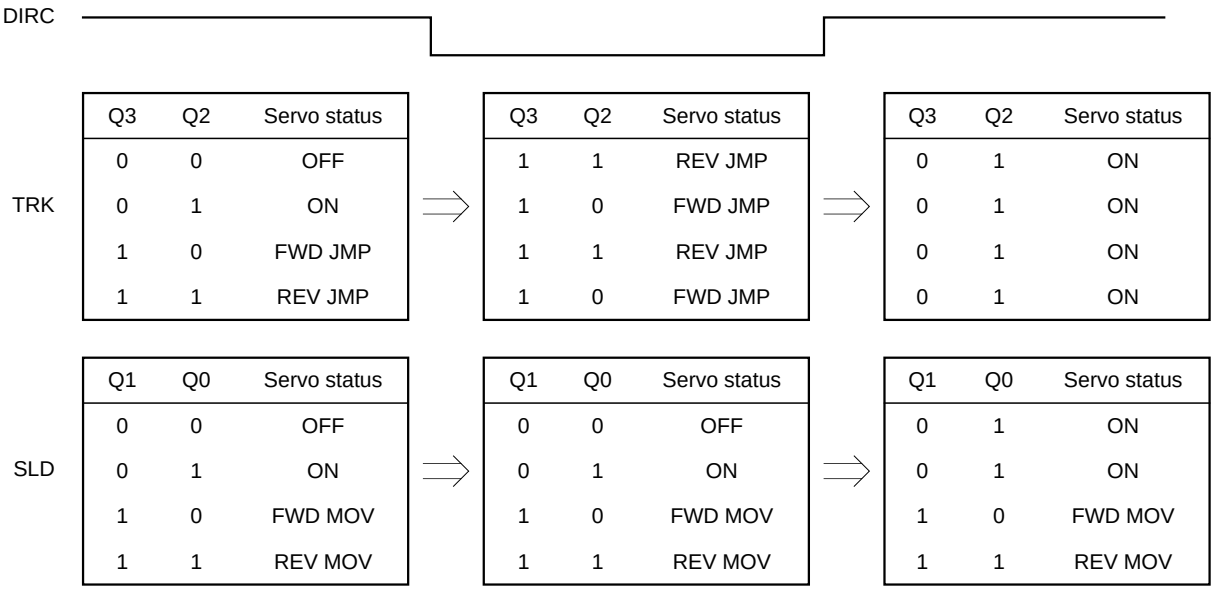


Fig. 3-22. Operational Amplifier Drive Circuit

§3-16. DIRC Input Pin

The $2 command register can be changed by operating the DIRC input pin (Pin 82).
Using the DIRC pin allows serial data transfer to be simplified during TRKJMP.
Fig. 3-23 shows $2 command register changes produced by DIRC pin changes.
In addition, Timing Chart 3-24 shows DIRC-based operations during TRKJMP.
High level must be input to the DIRC pin when the XRST pin rises from low to high.



Q3	Q2	Servo status
0	0	OFF
0	1	ON
1	0	FWD JMP
1	1	REV JMP

Q3	Q2	Servo status
1	1	REV JMP
1	0	FWD JMP
1	1	REV JMP
1	0	FWD JMP

Q3	Q2	Servo status
0	1	ON
0	1	ON
0	1	ON
0	1	ON

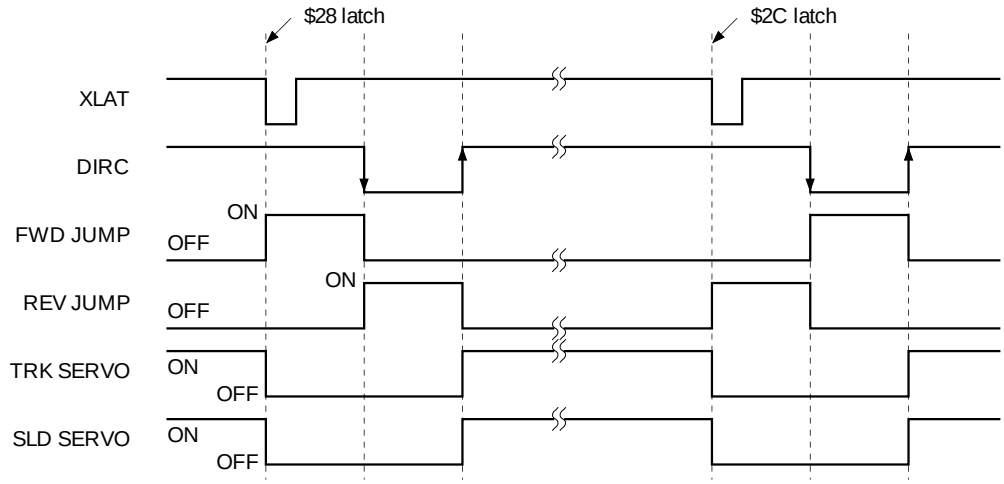
Q1	Q0	Servo status
0	0	OFF
0	1	ON
1	0	FWD MOV
1	1	REV MOV

Q1	Q0	Servo status
0	0	OFF
0	1	ON
1	0	FWD MOV
1	1	REV MOV

Q1	Q0	Servo status
0	1	ON
0	1	ON
1	0	FWD MOV
1	1	REV MOV

Q3, Q2, Q1 and Q0 correspond to D19, D18, D17 and D16 of $2.

Fig. 3-23.



Timing Chart 3-24.

§3-17. Servo Status Changes Produced by the LOCK Signal

When the LOCK signal becomes low, the TRK servo assumes the gain-up status and the SLD servo turns off in order to prevent SLD free-running.
Setting D6 (LKSW) of $38 to 1 deactivates this function.
In other words, neither the TRK servo nor the SLD servo change even when the LOCK signal becomes low.
This enables microcomputer control.

§3-18. Description of Commands and Data Sets

The following description contains portions which convert internal voltages into the values when they are output externally and describe them as input conversion or output conversion.
Input conversion converts these voltages into the voltages entering input pins before A/D conversion.
Output conversion converts PWM output values into analog voltage values.
Both types of conversion are calculated at V_{DD} = 5.0V. If this voltage changes, the conversion values also change proportionally. (Voltage conversion = V_{DDX}/5; V_{DDX}: used supply voltage)

$34

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	KA6	KA5	KA4	KA3	KA2	KA1	KA0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0

When D15 = 0.
KA6 to KA0: Coefficient address
KD7 to KD0: Coefficient data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	1	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	—

When D15 = D14 = D13 = D12 = 1. ($34F)
D11 = 0, D10 = 1
FBIAS register write
FB9 to FB1: Data; FB9 is MSB two's complement data.
For FE input conversion, FB9 to FB1 = 011111111 corresponds to +1V and FB9 to FB1 = 100000000 to –1V respectively. (when the supply voltage = 5V)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	0	TV9	TV8	TV7	TV6	TV5	TV4	TV3	TV2	TV1	TV0

When D15 = D14 = D13 = D12 = 1. ($34F)
D11 = 0, D10 = 0
TRVSC register write
TV9 to TV0: Data; TV9 is MSB two's complement data.
For TE input conversion, TV9 to TV0 = 0011111111 corresponds to +1V and TV9 to TV0 = 1100000000 to –1V respectively. (when the supply voltage = 5V)

Note)
- When the TRVSC register is read out, the data length is 9 bits. At this time, data corresponding to each bit of TV8 to TV0 during external write are read out.
- When reading out internally measured values and then writing these values externally, set TV9 the same as TV8.

$35

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FT1	FT0	FS5	FS4	FS3	FS2	FS1	FS0	FTZ	FG6	FG5	FG4	FG3	FG2	FG1	FG0

FT1, FT0, FTZ: Focus search-up speed

Default value: 010 (3.36V/s)

Focus drive output conversion

FT1	FT0	FTZ	Focus search speed
0	0	0	6.73 V/s
0	1	0	3.36
1	0	0	2.24
1	1	0	1.68
0	0	1	8.97
0	1	1	5.38
1	0	1	4.49
1	1	1	3.85

FS5 to FS0: Focus search limit voltage

Default value: 011000 (±1.875V)

Focus drive output conversion

FG6 to FG0: AGF convergence gain setting value

Default value: 0101101

$36

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	DTZC	TJ5	TJ4	TJ3	TJ2	TJ1	TJ0	0	TG6	TG5	TG4	TG3	TG2	TG1	TG0

DTZC: DTZC delay (8.5/4.25µs)

Default value: 0 (4.25µs)

TJ5 to TJ0: Track jump voltage

Default value: 001110 (≈ ±1.09V)

Tracking drive output conversion

TG6 to TG0: AGT convergence gain setting value

Default value: 0101110

$37

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FZSH	FZSL	SM5	SM4	SM3	SM2	SM1	SM0	AGS	AGJ	AGGF	AGGT	AGV1	AGV2	AGHS	AGHT

FZSH, FZSL: FZC (Focus Zero Cross) slice level
Default value: 01 (+250mV); FE input conversion

FZSH	FZSL	Slice level
0	0	+500mV
0	1	+250
1	0	+125
1	1	+62.5

SM5 to SM0: Sled move voltage
Default value: 010000 (≈ ±1.25V)
Sled drive output conversion

AGS: AGCNTL self-stop on/off
Default value: 1 (on)

AGJ: AGCNTL convergence completion judgment time during low sensitivity adjustment (31/63ms)
Default value: 0 (63ms)

AGGF: Focus AGCNTL internally generated sine wave amplitude (small/large)
Default value: 1 (large)

AGGT: Tracking AGCNTL internally generated sine wave amplitude (small/large)
Default value: 1 (large)

		FE/TE input conversion
AGGF	0 (small) 1 (large)	63mV 125
AGGT	0 (small) 1 (large)	125mV 250

AGV1: AGCNTL convergence sensitivity during high sensitivity adjustment; high/low
Default value: 1 (high)

AGV2: AGCNTL convergence sensitivity during low sensitivity adjustment; high/low
Default value: 0 (low)

AGHS: AGCNTL high sensitivity adjustment on/off
Default value: 1 (on)

AGHT: AGCNTL high sensitivity adjustment time (128/256ms)
Default value: 0 (256ms)

$38

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VCLM	VCLC	FLM	FLC0	RFLM	RFLC	AGF	AGT	DFSW	LKSW	TBLM	TCLM	FLC1	TLC2	TLC1	TLC0

◎ VCLM: VC level measurement (on/off)
VCLC: VC level compensation for FCS In register (on/off)
◎ FLM: Focus zero level measurement (on/off)
FLC0: Focus zero level compensation for FZC register (on/off)
◎ RFLM: RF zero level measurement (on/off)
RFLC: RF zero level compensation (on/off)
AGF: Focus automatic gain adjustment (on/off)
AGT: Tracking automatic gain adjustment (on/off)
DFSW: Defect disable switch (on/off)
Setting this switch to 1(on) disables the defect countermeasure circuit.
LKSW: Lock switch (on/off)
Setting this switch to 1 disables the sled free-running prevention circuit.
TBLM: Traverse center measurement (on/off)
◎ TCLM: Tracking zero level measurement (on/off)
FLC1: Focus zero level compensation for FCS In register (on/off)
TLC2: Traverse center compensation (on/off)
TLC1: Tracking zero level compensation (on/off)
TLC0: VC level compensation for TRK/SLD In register (on/off)

Note) Commands marked with ◎ are accepted every 2.9ms.
All commands are on when set to 1.

$39

D15	D14	D13	D12	D11	D10	D9	D8
DAC	SD6	SD5	SD4	SD3	SD2	SD1	SD0

DAC: Serial data readout DAC mode (on/off)

SD6 to SD0: Serial readout data select

SD6	SD5	Readout data			Readout data length
1	Address = coefficient RAM data for (SD5 to SD0)				8 bit
0	1	Address = Data RAM data for (SD4 to SD0)			16 bit
0	0	SD4	SD3 to SD0		
		1	1 1 1 1	RF AVRG register	8 bit
			1 1 1 0	RFDC input signal	8 bit
			1 1 0 1	FBIAS register	9 bit
			1 1 0 0	TRVSC register	9 bit
			0 0 1 1	RFDC envelope (bottom)	8 bit
			0 0 1 0	RFDC envelope (peak)	8 bit
		0	1 1 ∗ ∗	VC AVRG register	9 bit
			1 0 ∗ ∗	FE AVRG register	9 bit
			0 1 ∗ ∗	TE AVRG register	9 bit
			0 0 1 1	FE input signal	8 bit
			0 0 1 0	TE input signal	8 bit
			0 0 0 1	SE input signal	8 bit
			0 0 0 0	VC input signal	8 bit

Note) Coefficients K40 to K4F cannot be read out. ∗: Don't care

See the description for SRO1 and SRO0 of $3F concerning readout methods for the above data.

$3A

FBON: FBIAS (focus bias) register addition (on/off)

The FBIAS register value is added to the signal loaded into the FCS In register by setting D14 to 1 (on).

$3B

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4
SFO2	SFO1	SDF2	SDF1	MAX2	MAX1	SFOX	BTF	D2V2	D2V1	D1V2	D1V1

SFOX, SFO2, SFO1: FOK slice level

Default value: 011 (313mV)

RFDC input conversion

SFOX	SFO2	SFO1	Slice level
0	0	0	179mV
0	0	1	223
0	1	0	268
0	1	1	313
1	0	0	357
1	0	1	446
1	1	0	536
1	1	1	625

SDF2, SDF1: DFCT slice level
Default value: 10 (179 mV)
RFDC input conversion

SDF2	SDF1	Slice level
0	0	89mV
0	1	134
1	0	179
1	1	224

MAX2, MAX1: DFCT maximum time
Default value: 00 (no timer limit)

MAX2	MAX1	DFCT maximum time
0	0	No timer limit
0	1	2.00ms
1	0	2.36
1	1	2.72

BTF: Bottom hold double-speed count-up mode for MIRR signal generation
On/off (default: off)
On when set to 1.

D2V2, D2V1: Peak hold 2 for DFCT signal generation
Count-down speed setting
Default value: 01 (0.492V/ms, 44.1kHz)
[V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

D2V2	D2V1	Count-down speed	
		[V/ms]	[kHz]
0	0	0.246	22.05
0	1	0.492	44.1
1	0	0.984	88.2
1	1	1.969	176.4

D1V2, D1V1: Peak hold 1 for DFCT signal generation
Count down speed setting
Default value: 01 (3.938V/ms, 352.8kHz)
[V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

D1V2	D1V1	Count-down speed	
		[V/ms]	[kHz]
0	0	1.969	176.4
0	1	3.938	352.8
1	0	7.875	705.6
1	1	15.75	1411.2

$3E

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5
F1NM	F1DM	F3NM	F3DM	T1NM	T1UM	T3NM	T3UM	DFIS	TLCD	RFLP

F1NM, F1DM: Quasi double accuracy setting for FCS servo filter first-stage
On when set to 1; default = 0.
F1NM: Gain normal
F1DM: Gain down

T1NM, T1UM: Quasi double accuracy setting for TRK servo filter first-stage
On when set to 1; default = 0.
T1NM: Gain normal
T1UM: Gain up

F3NM, F3DM: Quasi double accuracy setting for FCS servo filter third-stage
On when set to 1; default = 0.
Generally, the advance amount of the phase becomes large by partially setting the FCS servo third-stage filter which is used as the phase compensation filter to double accuracy.
F3NM: Gain normal
F3DM: Gain down

T3NM, T3UM: Quasi double accuracy setting for TRK servo filter third-stage
On when set to 1; default = 0.
Generally, the advance amount of the phase becomes large by partially setting the TRK servo third-stage filter which is used as the phase compensation filter to double accuracy.
T3NM: Gain normal
T3UM: Gain up

Note) Filter first- and third-stage quasi double accuracy settings can be set individually.
See FILTER Composition at the end of this specification concerning quasi double-accuracy.

DFIS: FCS hold filter input extraction node selection
0: M05 (Data RAM address 05); default
1: M04 (Data RAM address 04)

TLCD: This command masks the TLC2 command set by D2 of $38 only when FOK is low.
On when set to 1; default = 0
RFLP: This command passes the signal obtained from the RFDC pin through the LPF (low-pass filter) before the built-in A/D converter.
0: LPF off; default
1: LPF on

$3F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	XT4D	XT2D	0	DRR2	DRR1	DRR0	0	ASFG	0	LPAS	SRO1	SRO0	0	0

XT4D, XT2D: MCK (digital servo master clock) frequency division setting

This command forcibly sets the frequency division ratio to 1/4 or 1/2 when MCK is generated from the signal input to the FSTI pin.

XT4D	XT2D	Frequency division ratio
0	0	According to XTSL (default)
0	1	1/2
1	0	1/4

DRR2 to DRR0: Partially clears the Data RAM values (0 write).

The following values are cleared when set to 1 (on) respectively; default = 0

DRR2: M08, M09, M0A

DRR1: M00, M01, M02

DRR0: M00, M01, M02 only when LOCK = low

Note) Set DRR1 and DRR0 so that they are on continuously for 50µs or more.

ASFG: When vibration detection is performed during anti-shock circuit operation, the TRK servo filter is set to the gain-up status, and forcibly FCS servo filter to gain normal status.

On when set to 1; default = 0

LPAS: Built-in analog buffer low-current consumption mode

This mode suppresses the total analog buffer current consumption for the VC, TE, SE and FE input analog buffers by using a single operational amplifier.

On when set to 1; default = 0

Note) When using this mode, first check whether each error signal is being properly A/D converted using the SRO1 and SRO0 commands of $3F.

SRO1, SRO0: These commands are used to continuously externally output various data in the digital servo block which have been specified with the $39 command. (However, D15 (DAC) of $39 must be set to 1.)

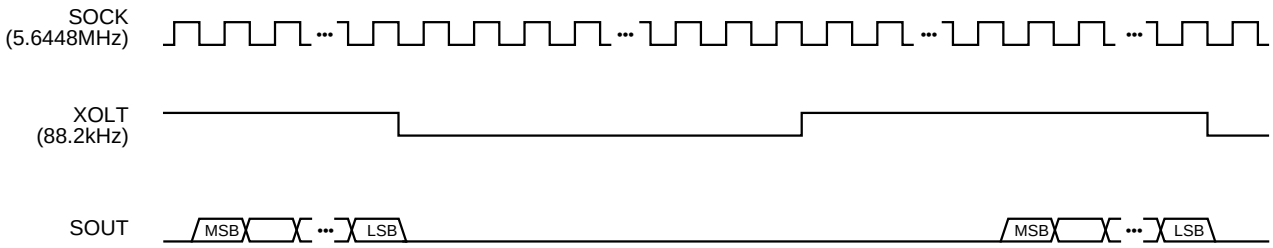
Digital output can be obtained from three specified pins (SOCK, XOLT and SOUT) by setting these commands to 1 respectively. The default is 0, 0.

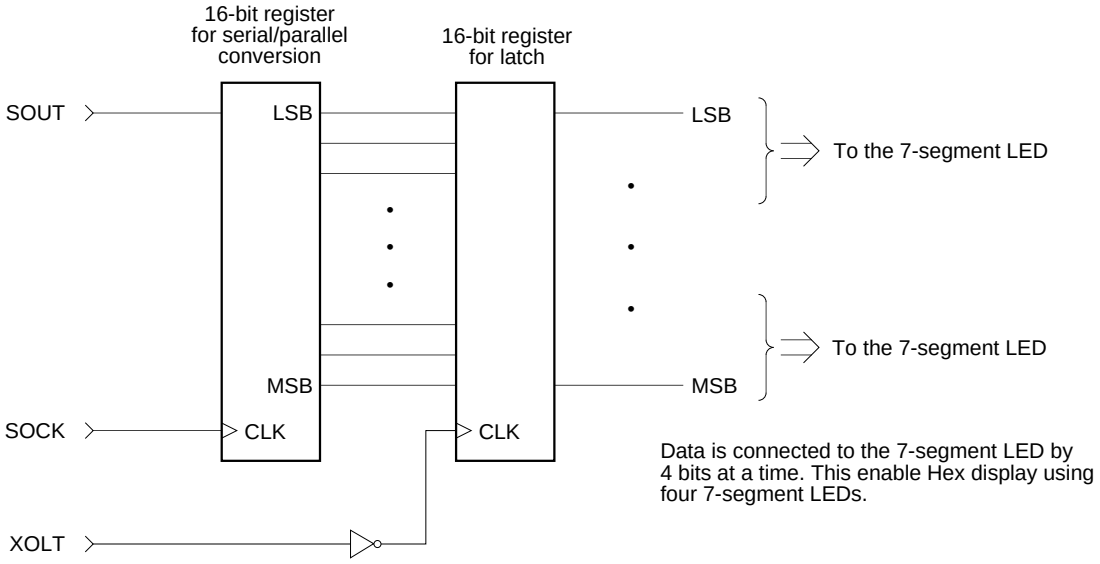
The output pins for each case are shown below.

	SRO1 = 1	SRO0 = 1
SOCK	DA13 (49)	DA10 (52)
XOLT	DA12 (50)	DA09 (53)
SOUT	DA14 (48)	DA11 (51)

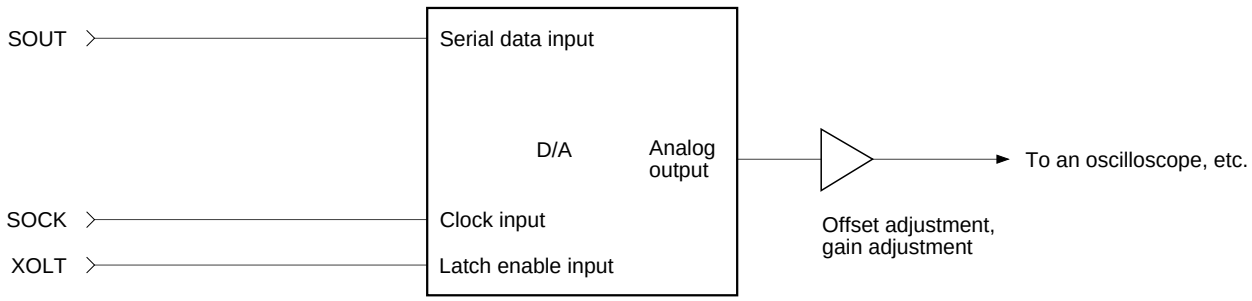
(See the Description of Data Readout on the following page.)

Description of Data Readout





Data is connected to the 7-segment LED by 4 bits at a time. This enable Hex display using four 7-segment LEDs.



Waveforms can be monitored with an oscilloscope using a serial input-type D/A converter as shown above.

§3-19. List of Servo Filter Coefficients

<Coefficient Preset Value Table (1)>

ADDRESS	DATA	CONTENTS
K00	E0	SLED INPUT GAIN
K01	81	SLED LOW BOOST FILTER A-H
K02	23	SLED LOW BOOST FILTER A-L
K03	7F	SLED LOW BOOST FILTER B-H
K04	6A	SLED LOW BOOST FILTER B-L
K05	10	SLED OUTPUT GAIN
K06	14	FOCUS INPUT GAIN
K07	30	SLED AUTO GAIN
K08	7F	FOCUS HIGH CUT FILTER A
K09	46	FOCUS HIGH CUT FILTER B
K0A	81	FOCUS LOW BOOST FILTER A-H
K0B	1C	FOCUS LOW BOOST FILTER A-L
K0C	7F	FOCUS LOW BOOST FILTER B-H
K0D	58	FOCUS LOW BOOST FILTER B-L
K0E	82	FOCUS PHASE COMPENSATE FILTER A
K0F	7F	FOCUS DEFECT HOLD GAIN
K10	4E	FOCUS PHASE COMPENSATE FILTER B
K11	32	FOCUS OUTPUT GAIN
K12	20	ANTI SHOCK INPUT GAIN
K13	30	FOCUS AUTO GAIN
K14	80	HPTZC / Auto Gain HIGH PASS FILTER A
K15	77	HPTZC / Auto Gain HIGH PASS FILTER B
K16	80	ANTI SHOCK HIGH PASS FILTER A
K17	77	HPTZC / Auto Gain LOW PASS FILTER B
K18	00	Fix*
K19	F1	TRACKING INPUT GAIN
K1A	7F	TRACKING HIGH CUT FILTER A
K1B	3B	TRACKING HIGH CUT FILTER B
K1C	81	TRACKING LOW BOOST FILTER A-H
K1D	44	TRACKING LOW BOOST FILTER A-L
K1E	7F	TRACKING LOW BOOST FILTER B-H
K1F	5E	TRACKING LOW BOOST FILTER B-L
K20	82	TRACKING PHASE COMPENSATE FILTER A
K21	44	TRACKING PHASE COMPENSATE FILTER B
K22	18	TRACKING OUTPUT GAIN
K23	30	TRACKING AUTO GAIN
K24	7F	FOCUS GAIN DOWN HIGH CUT FILTER A
K25	46	FOCUS GAIN DOWN HIGH CUT FILTER B
K26	81	FOCUS GAIN DOWN LOW BOOST FILTER A-H
K27	3A	FOCUS GAIN DOWN LOW BOOST FILTER A-L
K28	7F	FOCUS GAIN DOWN LOW BOOST FILTER B-H
K29	66	FOCUS GAIN DOWN LOW BOOST FILTER B-L
K2A	82	FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
K2B	44	FOCUS GAIN DOWN DEFECT HOLD GAIN
K2C	4E	FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
K2D	1B	FOCUS GAIN DOWN OUTPUT GAIN
K2E	00	NOT USED
K2F	00	NOT USED

<Coefficient ROM Preset Value Table (2)>

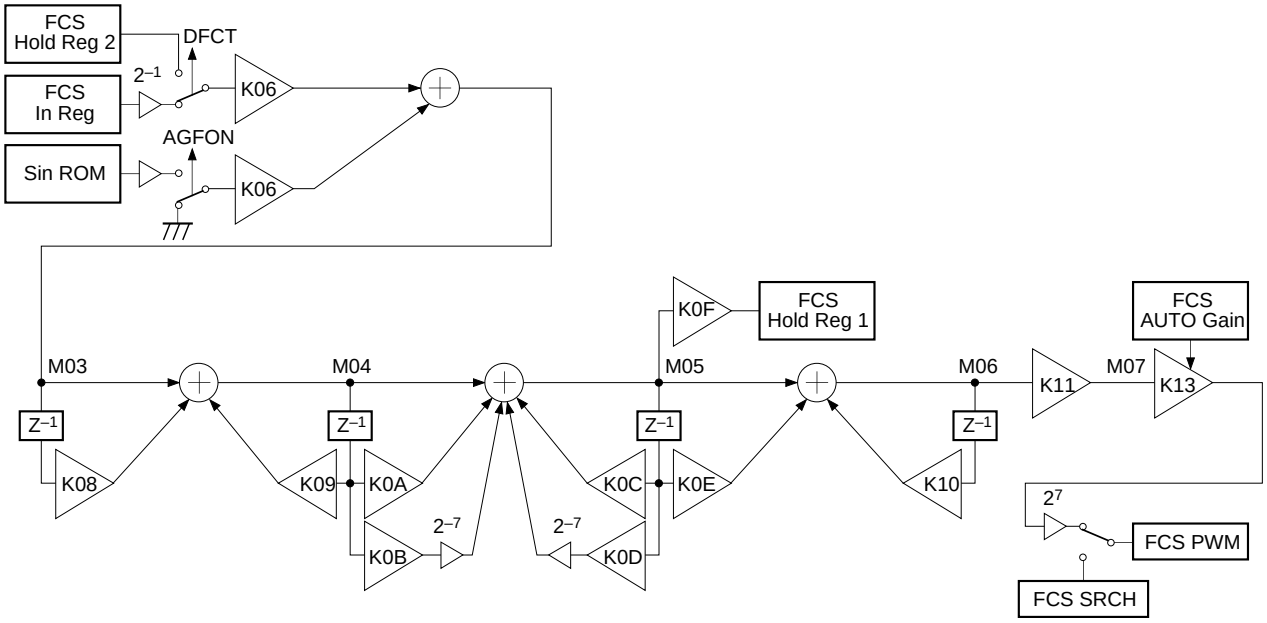
ADDRESS	DATA	CONTENTS
K30	80	Fix*
K31	66	ANTI SHOCK LOW PASS FILTER B
K32	00	NOT USED
K33	7F	ANTI SHOCK HIGH PASS FILTER B-H
K34	6E	ANTI SHOCK HIGH PASS FILTER B-L
K35	20	ANTI SHOCK FILTER COMPARATE GAIN
K36	7F	TRACKING GAIN UP2 HIGH CUT FILTER A
K37	3B	TRACKING GAIN UP2 HIGH CUT FILTER B
K38	80	TRACKING GAIN UP2 LOW BOOST FILTER A-H
K39	44	TRACKING GAIN UP2 LOW BOOST FILTER A-L
K3A	7F	TRACKING GAIN UP2 LOW BOOST FILTER B-H
K3B	77	TRACKING GAIN UP2 LOW BOOST FILTER B-L
K3C	86	TRACKING GAIN UP PHASE COMPENSATE FILTER A
K3D	0D	TRACKING GAIN UP PHASE COMPENSATE FILTER B
K3E	57	TRACKING GAIN UP OUTPUT GAIN
K3F	00	NOT USED
K40	04	TRACKING HOLD FILTER INPUT GAIN
K41	7F	TRACKING HOLD FILTER A-H
K42	7F	TRACKING HOLD FILTER A-L
K43	79	TRACKING HOLD FILTER B-H
K44	17	TRACKING HOLD FILTER B-L
K45	6D	TRACKING HOLD FILTER OUTPUT GAIN
K46	00	NOT USED
K47	00	NOT USED
K48	02	FOCUS HOLD FILTER INPUT GAIN
K49	7F	FOCUS HOLD FILTER A-H
K4A	7F	FOCUS HOLD FILTER A-L
K4B	79	FOCUS HOLD FILTER B-H
K4C	17	FOCUS HOLD FILTER B-L
K4D	54	FOCUS HOLD FILTER OUTPUT GAIN
K4E	00	NOT USED
K4F	00	NOT USED

* Fix indicates that normal preset values should be used.

§3-20. FILTER Composition

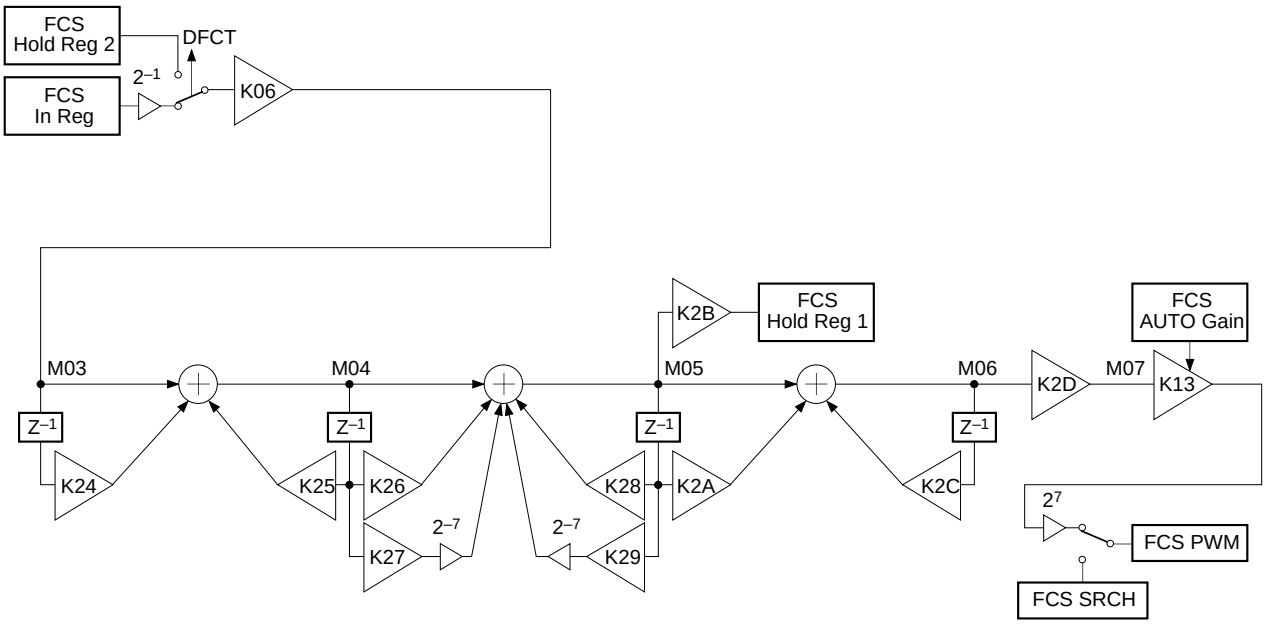
The internal filter composition is shown below.
K ∗ ∗ and M ∗ ∗ indicate coefficient RAM and Data RAM address values respectively.

FCS Servo Gain Normal; fs = 88.2kHz



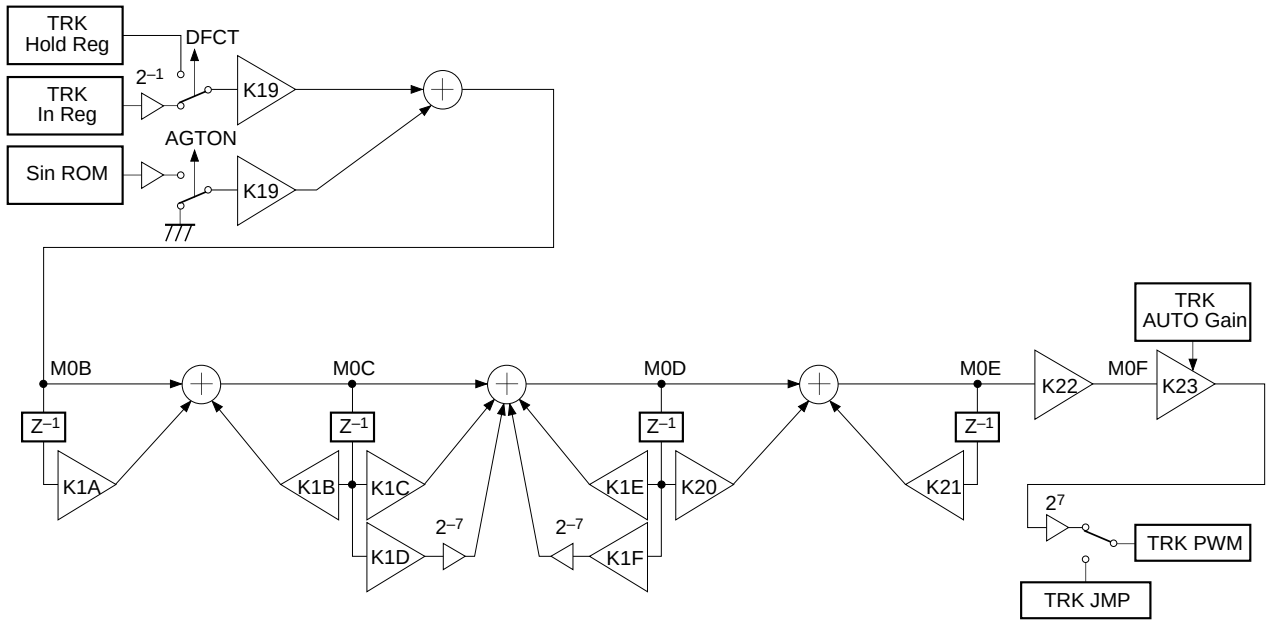
Note) Set the MSB bit of the K0B and K0D coefficients to 0.

FCS Servo Gain Down; fs = 88.2kHz



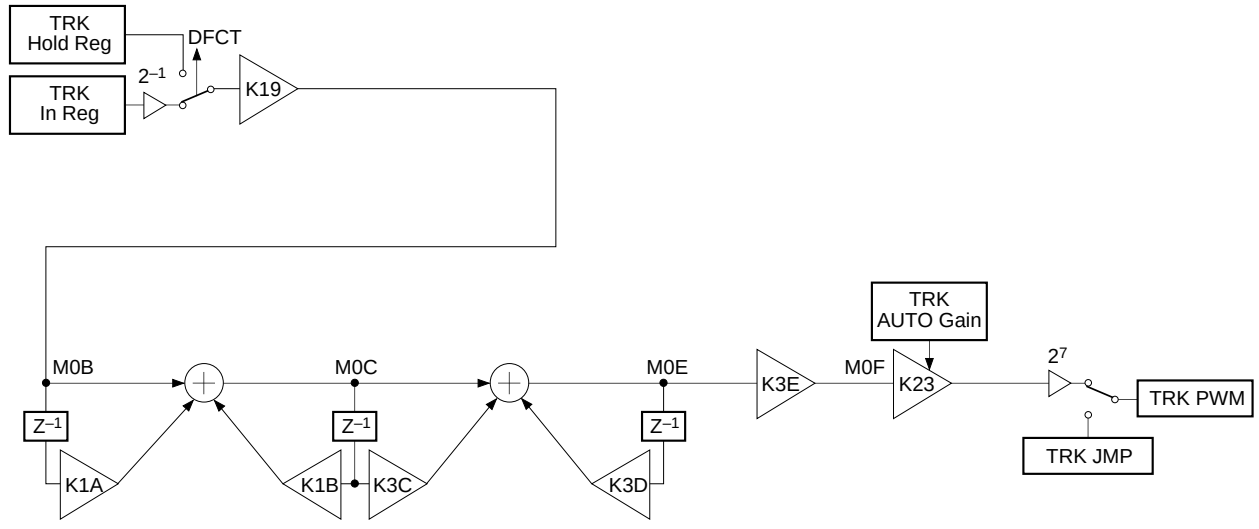
Note) Set the MSB bit of the K27 and K29 coefficients to 0.

TRK Servo Gain Normal; fs = 88.2kHz

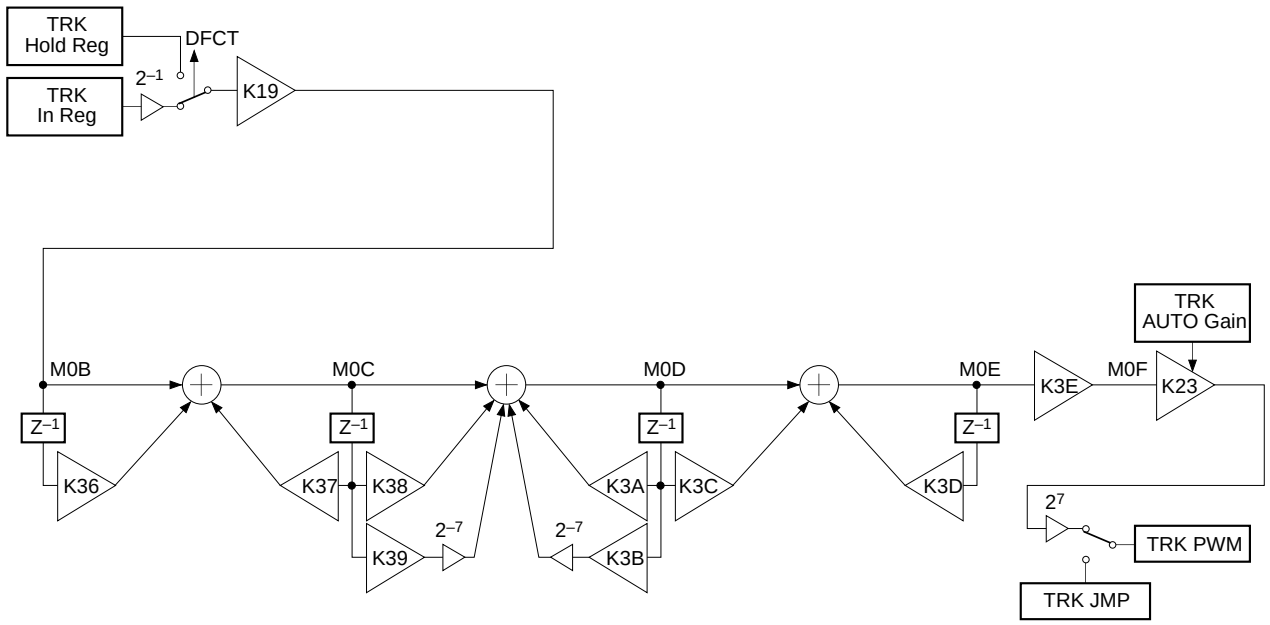


Note) Set the MSB bit of the K1D and K1F coefficients to 0.

TRK Servo Gain Up 1; fs = 88.2kHz

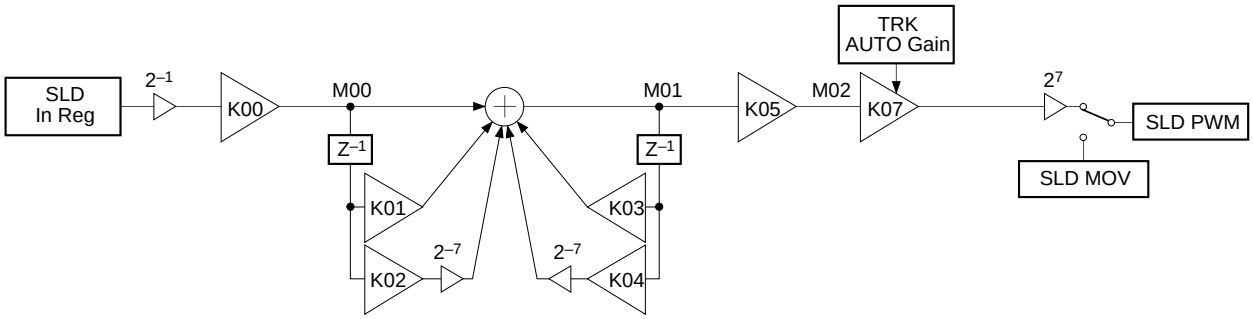


TRK Servo Gain Up 2; fs = 88.2kHz



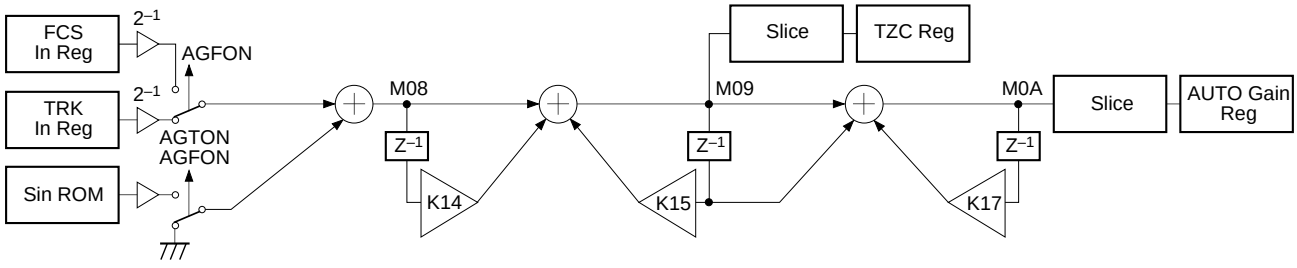
Note) Set the MSB bit of the K39 and K3B coefficients to 0.

SLD Servo; fs = 345Hz

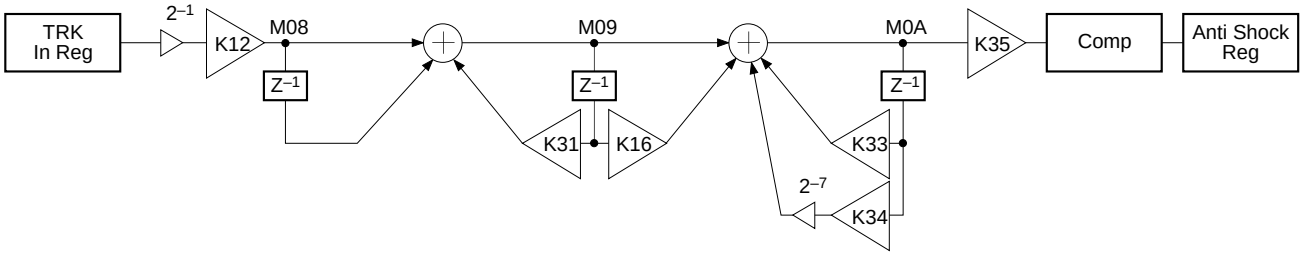


Note) Set the MSB bit of the K02 and K04 coefficients to 0.

HPTZC/Auto Gain; fs = 88.2kHz

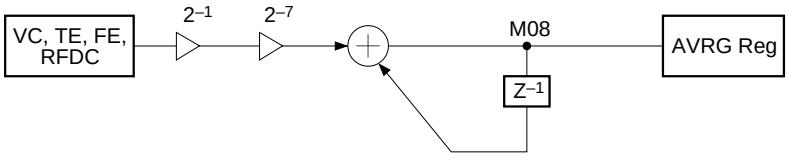


Anti Shock; fs = 88.2kHz

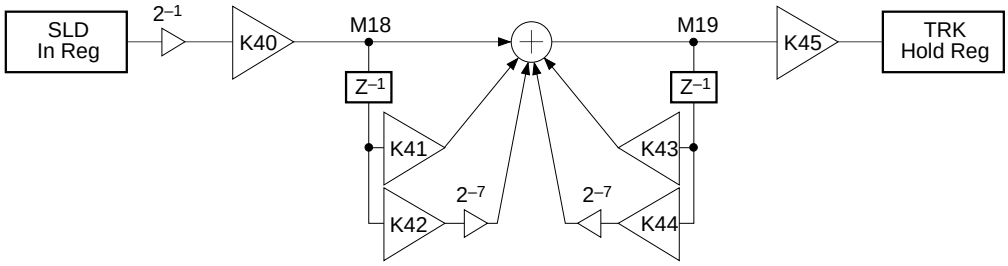


Note) Set the MSB bit of the K34 coefficient to 0.
The comparator level is 1/16 the maximum amplitude of the comparator input.

AVRG; fs = 88.2kHz

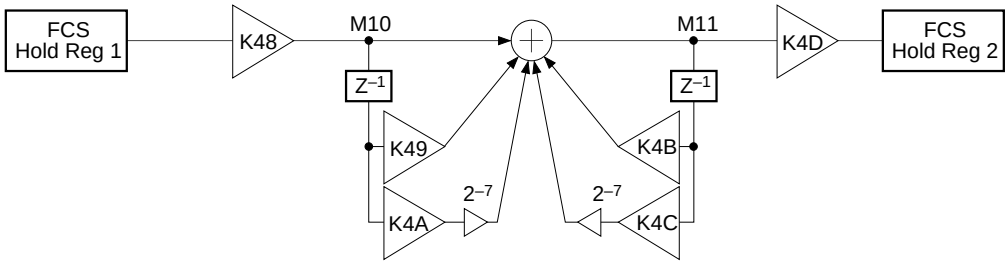


TRK Hold; fs = 345Hz



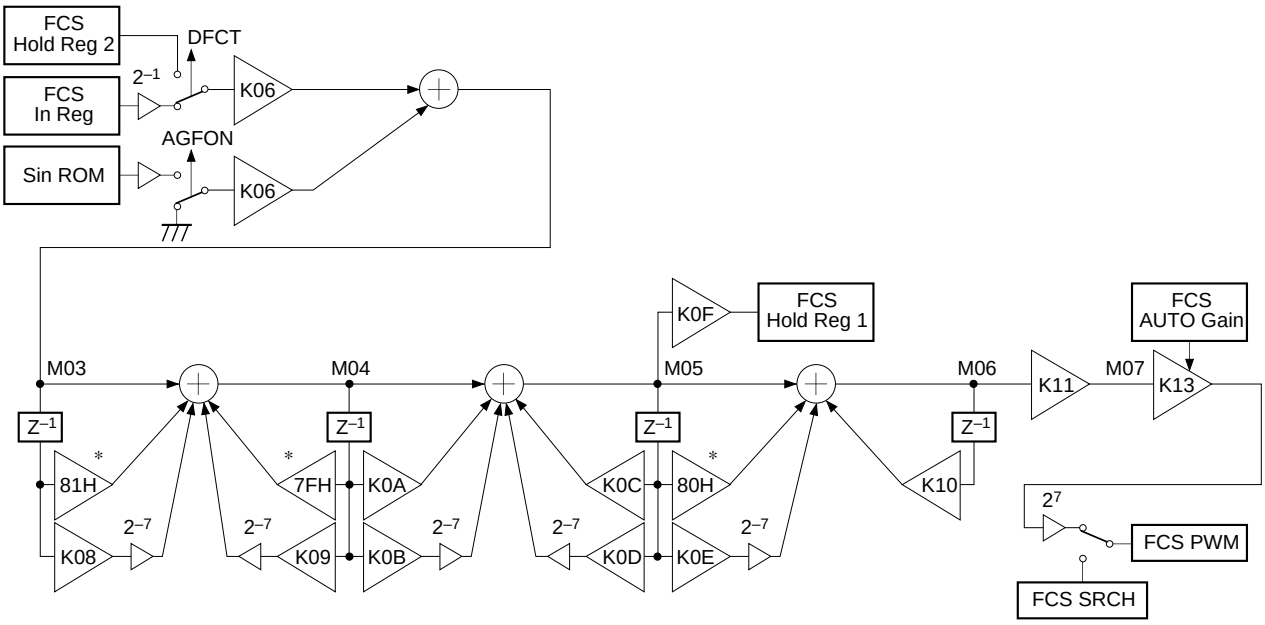
Note) Set the MSB bit of the K42 and K44 coefficients to 0.

FCS Hold; fs = 345Hz



Note) Set the MSB bit of the K4A and K4C coefficients to 0.

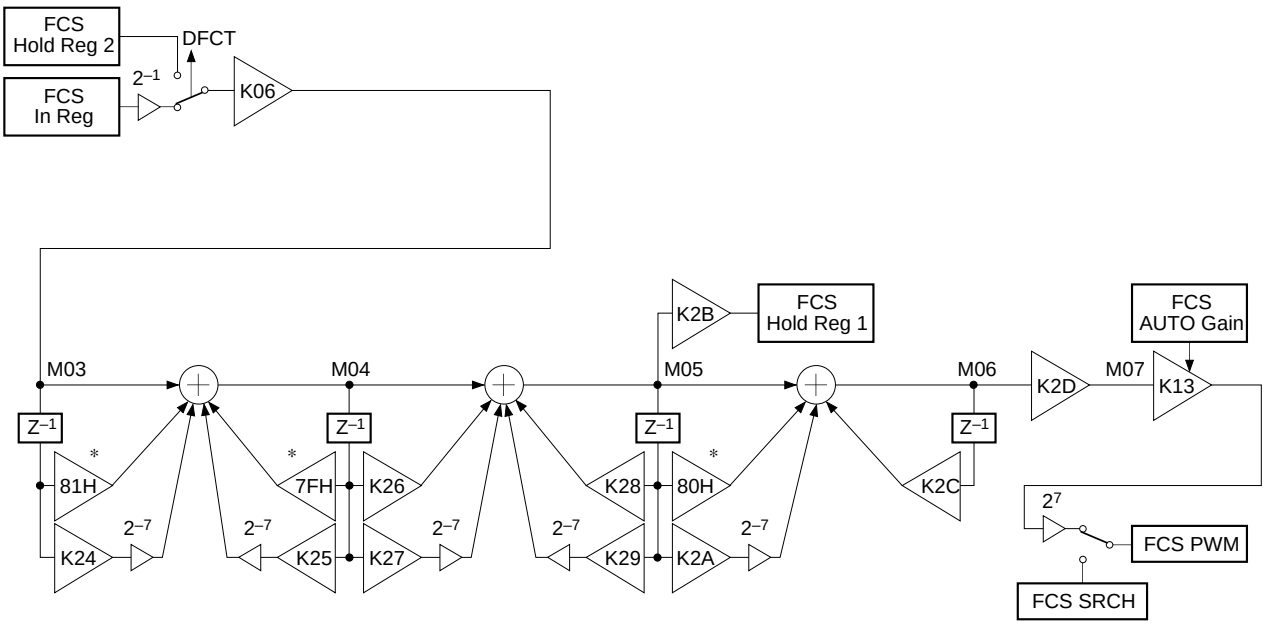
FCS Servo Gain Normal; fs = 88.2kHz, during quasi double accuracy (Ex.: $3EAXX0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K0B and K0D coefficients during normal operation, and of the K08, K09 and K0E coefficients during quasi double accuracy to 0.

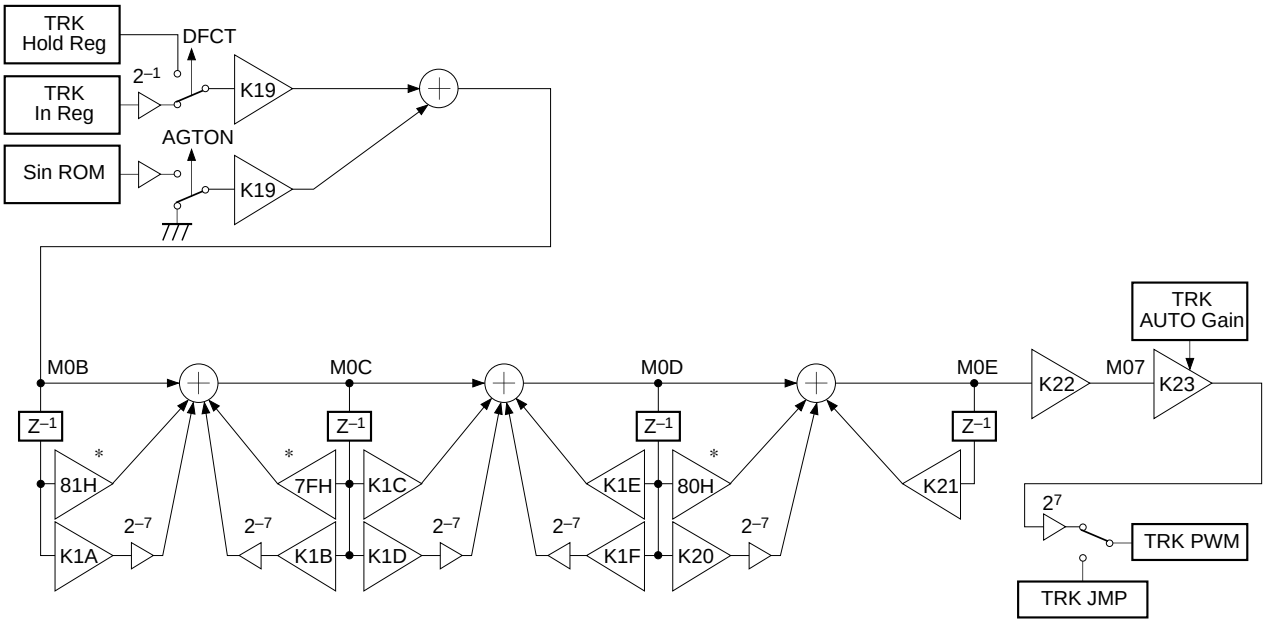
FCS Servo Gain Down; fs = 88.2kHz, during quasi double accuracy (Ex.: $3E5XX0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K27 and K29 coefficients during normal operation, and of the K24, K25 and K2A coefficients during quasi double accuracy to 0.

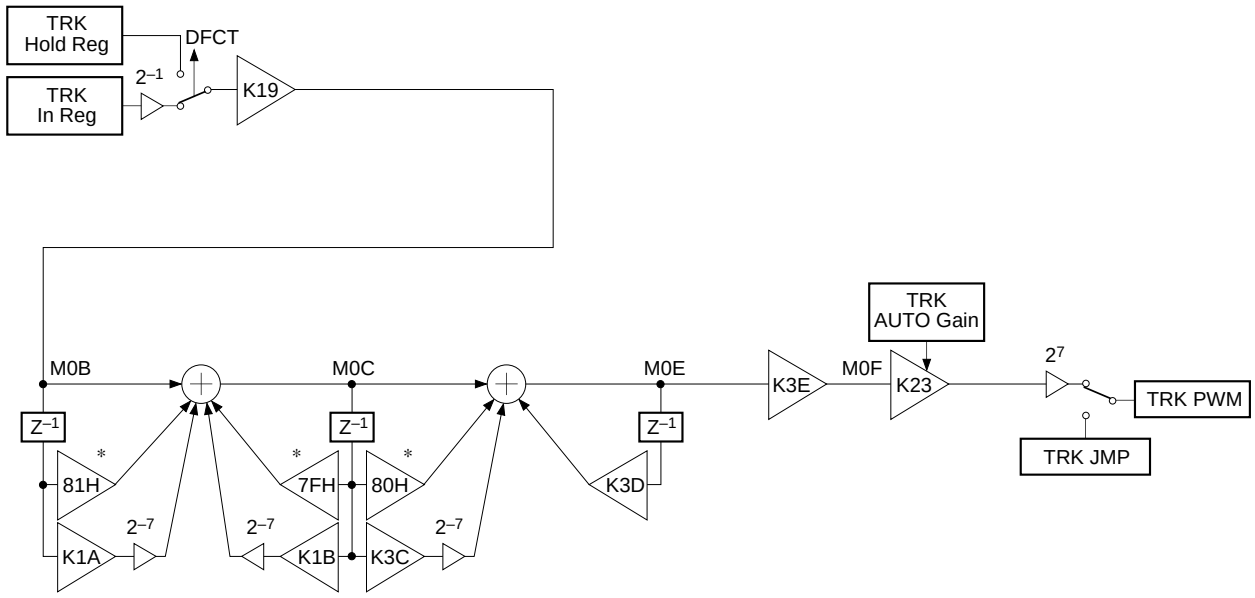
TRK Servo Gain Normal; fs = 88.2kHz, during quasi double accuracy (Ex.: $3EXAX0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K1D and K1F coefficients during normal operation, and of the K1A, K1B and K20 coefficients during quasi double accuracy to 0.

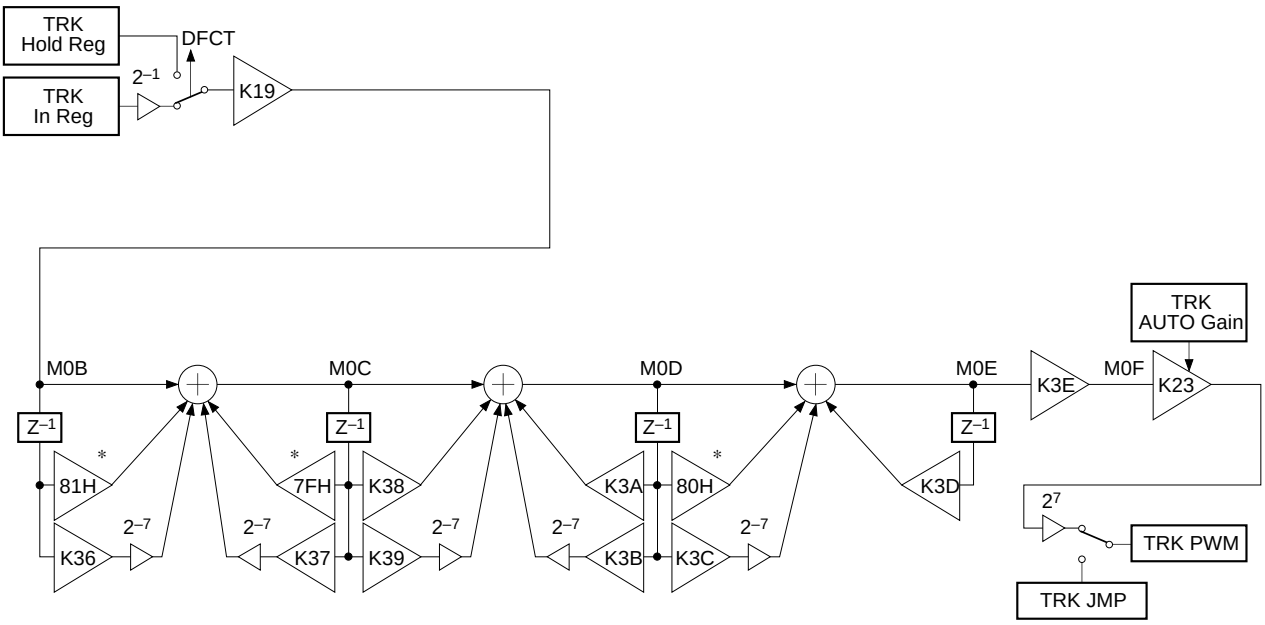
TRK Servo Gain up 1; fs = 88.2kHz, during quasi double accuracy (Ex.: $3EX5X0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K1A, K1B and K3C coefficients during quasi double accuracy to 0.

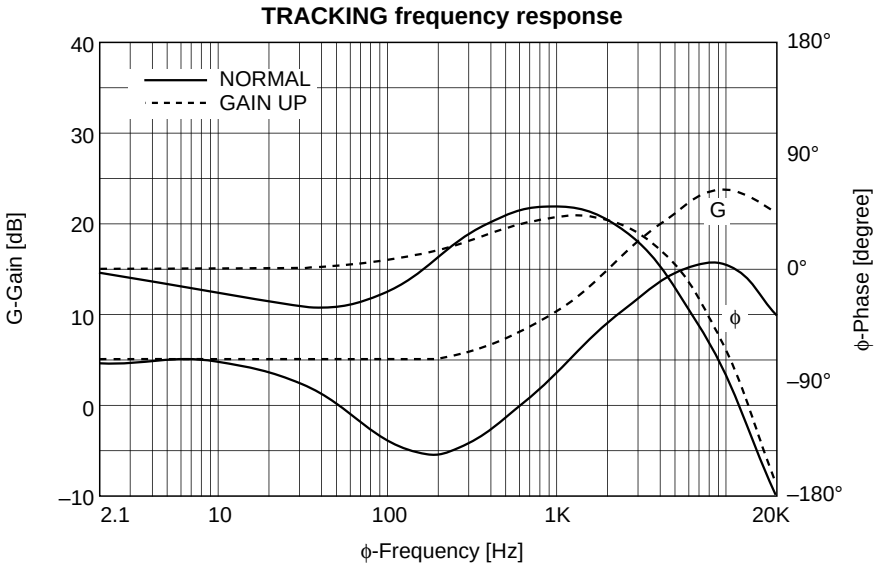
TRK Servo Gain up 2; fs = 88.2kHz, during quasi double accuracy (Ex.: $3EX5X0)

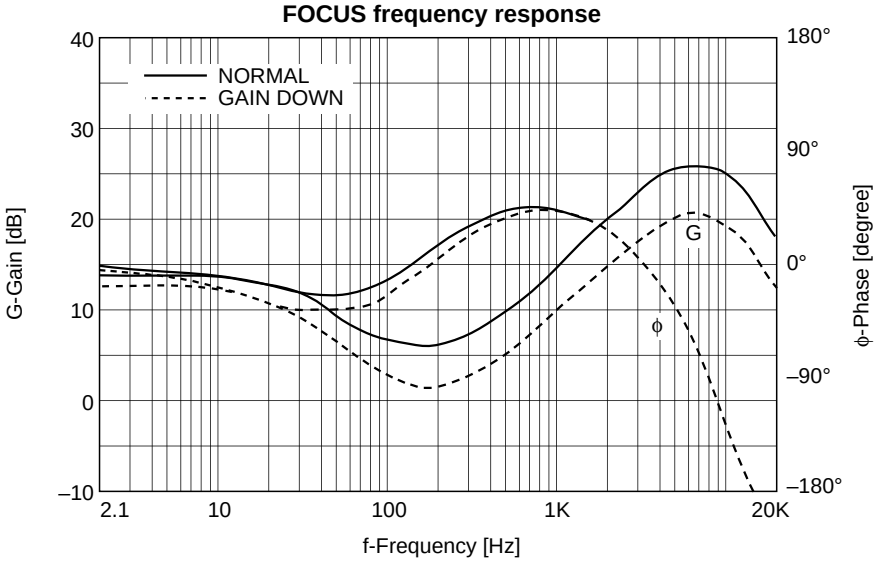


* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K39 and K3B coefficients during normal operation, and of the K36, K37 and K3C coefficients during quasi double accuracy to 0.

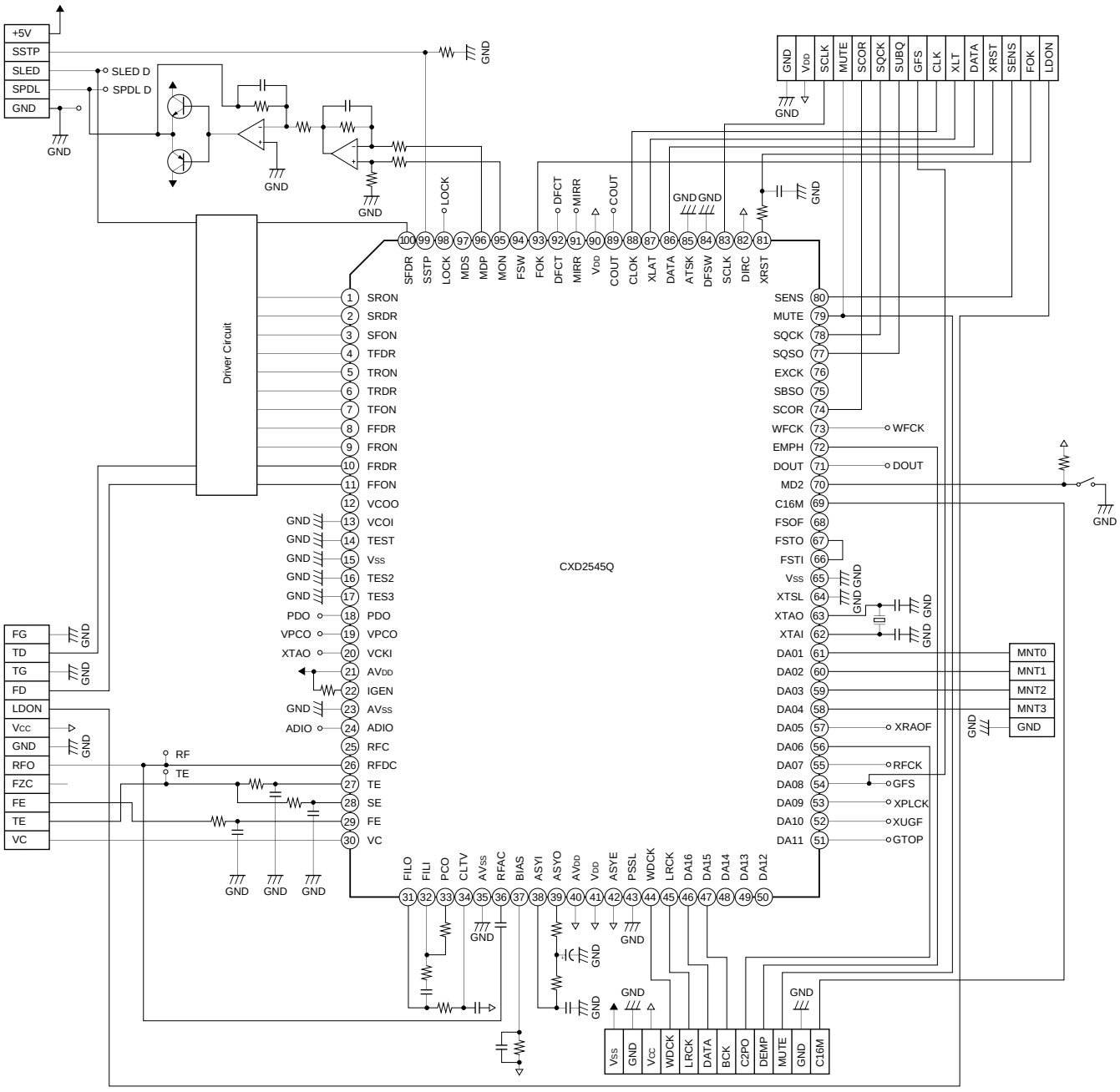
§3-21. TRACKING and FOCUS Frequency Response





[4] Application Circuit

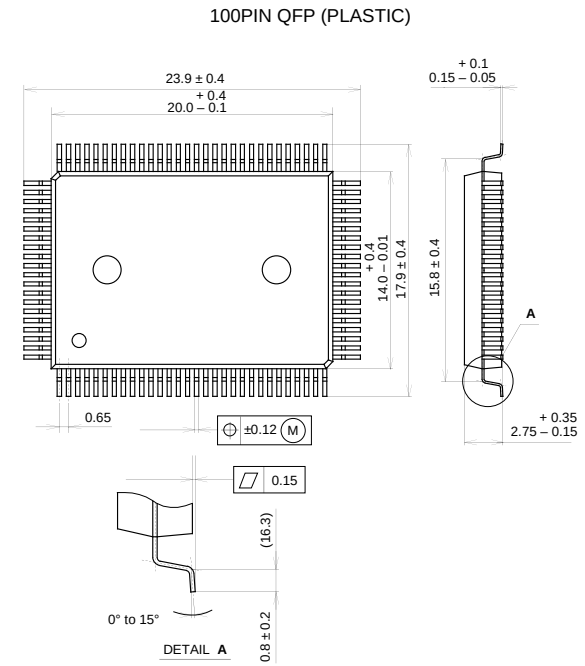
§4-1. Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

QFP-100P-L01

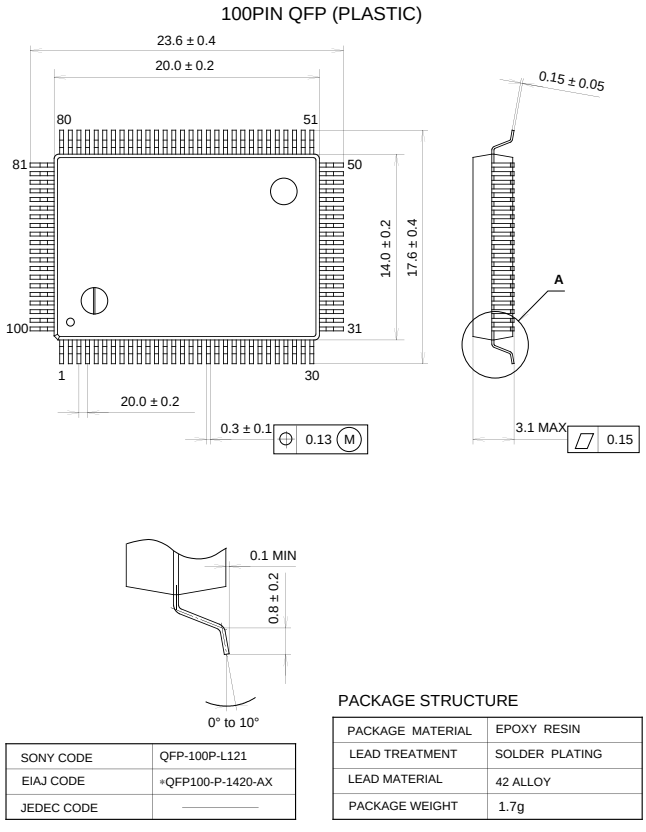


PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g

SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	

QFP-100P-L121



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.7g

SONY CODE	QFP-100P-L121
EIAJ CODE	*QFP100-P-1420-AX
JEDEC CODE	