



## 32K × 8 HIGH-SPEED CMOS STATIC RAM

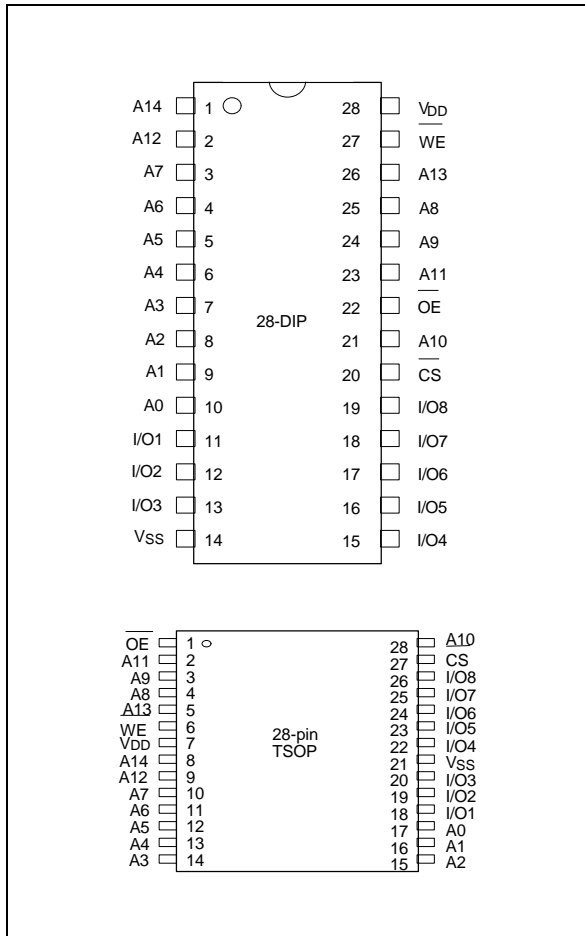
### GENERAL DESCRIPTION

The W24L257A is a high-speed, low-power CMOS static RAM organized as 32768 × 8 bits that operates on a single 3.3-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

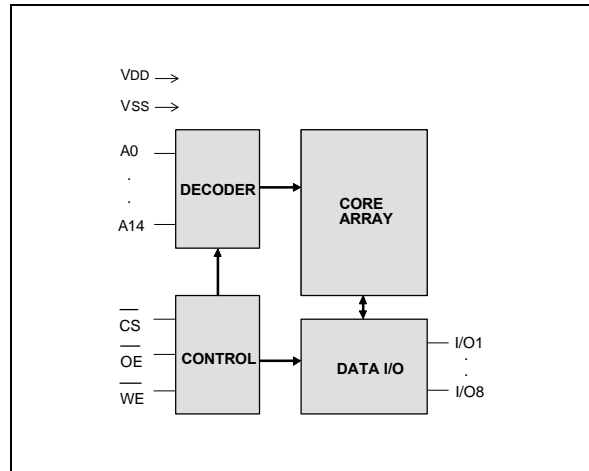
### FEATURES

- High-speed access time: 12/15/20 nS (max.)
- Low-power consumption:
  - Active: 200 mW (typ.)
- Single +3.3V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Available packages: 28-pin 300 mil SOJ, skinny DIP and standard type one TSOP (8 mm × 13.4 mm)

### PIN CONFIGURATION



### BLOCK DIAGRAM



### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A14	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
$\overline{\text{CS}}$	Chip Select Input
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{OE}}$	Output Enable Input
VDD	Power Supply
VSS	Ground



## TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O1–I/O8	V <sub>DD</sub> CURRENT
H	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	Output Disable	High Z	I <sub>DD</sub>
L	L	H	Read	Data Out	I <sub>DD</sub>
L	X	L	Write	Data In	I <sub>DD</sub>

## DC CHARACTERISTICS

### Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V <sub>SS</sub> Potential	-0.5 to +4.6	V
Input/Output to V <sub>SS</sub> Potential	-0.5 to V <sub>DD</sub> +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### Operating Characteristics

(V<sub>DD</sub> = 3.3V ± 5%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70° C)

PARAMETER	SYM	TEST CONDITIONS	MIN	TYP	MAX.	UNIT	
Input Low Voltage	V <sub>IL</sub>	-	-0.5	-	+0.8	V	
Input High Voltage	V <sub>IH</sub>	-	+2.0	-	V <sub>DD</sub> +0.3	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>DD</sub>	-10	-	+10	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>DD</sub> , $\overline{CS}$ = V <sub>IH</sub> (min.) or $\overline{OE}$ = V <sub>IH</sub> (min.) or $\overline{WE}$ = V <sub>IL</sub> (max.)	-10	-	+10	μA	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = +8.0 mA	-	-	0.4	V	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0 mA	2.4	-	-	V	
Operating Power	I <sub>DD</sub>	$\overline{CS}$ = V <sub>IL</sub> (max.), I/O = 0 mA	12	-	-	150	mA
Supply Current		Cycle = min. Duty = 100%	15	-	-	120	mA
			20	-	-	100	mA
Standby Power Supply Current	ISB	$\overline{CS}$ = V <sub>IH</sub> (min.), Cycle = min. Duty = 100%	-	-	20	mA	
	ISB1	$\overline{CS}$ ≥ V <sub>DD</sub> -0.2V	-	-	200	μA	

Note: Typical characteristics are at V<sub>DD</sub> = 3.3V, T<sub>a</sub> = 25° C.

## CAPACITANCE

(V<sub>DD</sub> = 3.3V, T<sub>a</sub> = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>OUT</sub> = 0V	8	pF

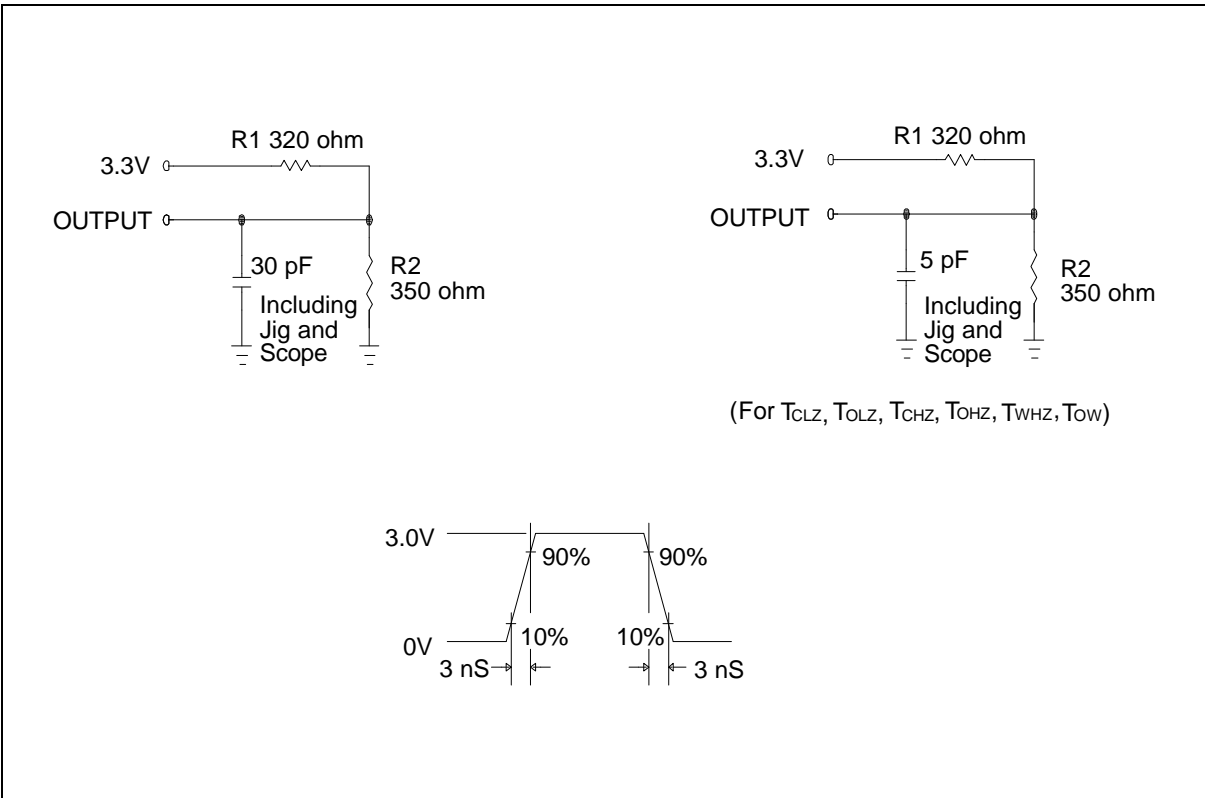
Note: These parameters are sampled but not 100% tested.

## AC CHARACTERISTICS

### AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 nS
Input and Output Timing Reference Level	1.5V
Output Load	C <sub>L</sub> = 30 pF, I <sub>OH</sub> /I <sub>OL</sub> = -4 mA/8 mA

### AC Test Loads and Waveform





AC Characteristics, continued  
(V<sub>DD</sub> = 3.3V ± 5%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70° C)

## (1) Read Cycle

PARAMETER	SYM.	W24L257A-12		W24L257A-15		W24L257A-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T <sub>RC</sub>	12	-	15	-	20	-	nS
Address Access Time	T <sub>AA</sub>	-	12	-	15	-	20	nS
Chip Select Access Time	T <sub>ACS</sub>	-	12	-	15	-	20	nS
Output Enable to Output Valid	T <sub>AOE</sub>	-	6	-	8	-	10	nS
Chip Selection to Output in Low Z	T <sub>CLZ</sub> *	4	-	4	-	4	-	nS
Output Enable to Output in Low Z	T <sub>OLZ</sub> *	0	-	0	-	0	-	nS
Chip Deselection to Output in High Z	T <sub>CHZ</sub> *	-	6	-	7	-	10	nS
Output Disable to Output in High Z	T <sub>OHZ</sub> *	-	6	-	7	-	10	nS
Output Hold from Address Change	T <sub>OH</sub>	3	-	3	-	3	-	nS

\*These parameters are sampled but not 100% tested

## (2) Write Cycle

PARAMETER	SYM.	W24L257A-12		W24L257A-15		W24L257A-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	T <sub>WC</sub>	12	-	15	-	20	-	nS
Chip Selection to End of Write	T <sub>CW</sub>	10	-	13	-	17	-	nS
Address Valid to End of Write	T <sub>AW</sub>	10	-	13	-	17	-	nS
Address Setup Time	T <sub>AS</sub>	0	-	0	-	0	-	nS
Write Pulse Width	T <sub>WP</sub>	10	-	10	-	12	-	nS
Write Recovery Time	$\overline{\text{CS}}, \overline{\text{WE}}$ T <sub>WR</sub>	1	-	1	-	1	-	nS
Data Valid to End of Write	T <sub>DW</sub>	7	-	9	-	10	-	nS
Data Hold from End of Write	T <sub>DH</sub>	0	-	0	-	0	-	nS
Write to Output in High Z	T <sub>WHZ</sub> *	-	7	-	8	-	10	nS
Output Disable to Output in High Z	T <sub>OHZ</sub> *	-	7	-	8	-	10	nS
Output Active from End of Write	T <sub>OW</sub>	0	-	0	-	0	-	nS

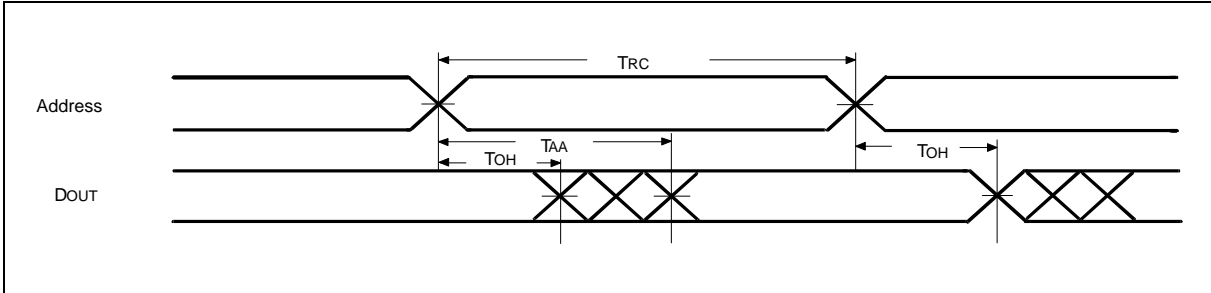
\*These parameters are sampled but not 100% tested



**TIMING WAVEFORMS**

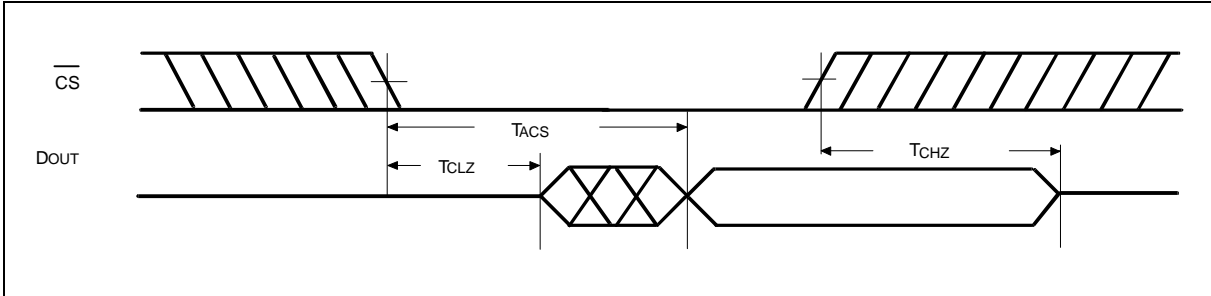
**Read Cycle 1**

(Address Controlled)



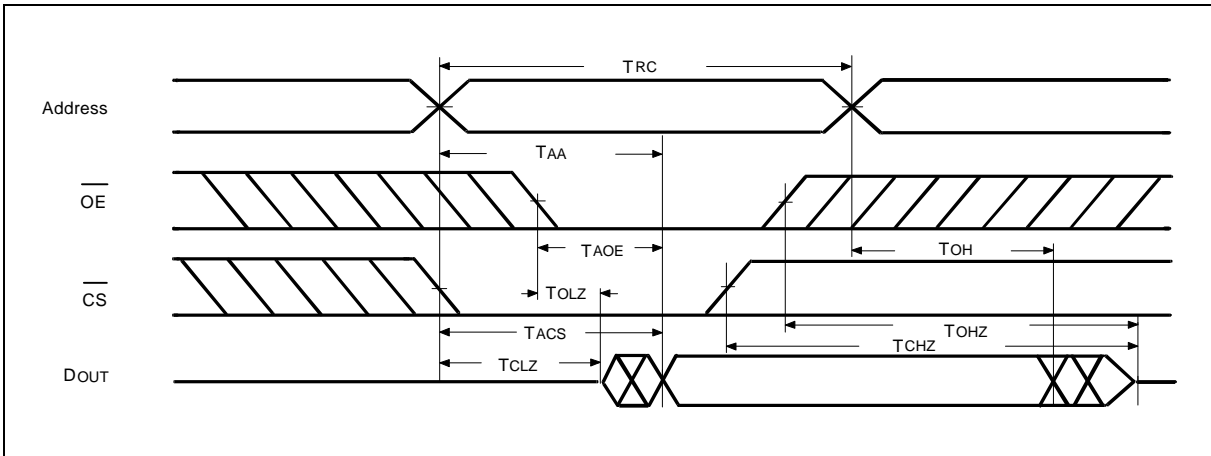
**Read Cycle 2**

(Chip Select Controlled)



**Read Cycle 3**

(Output Enable Controlled)

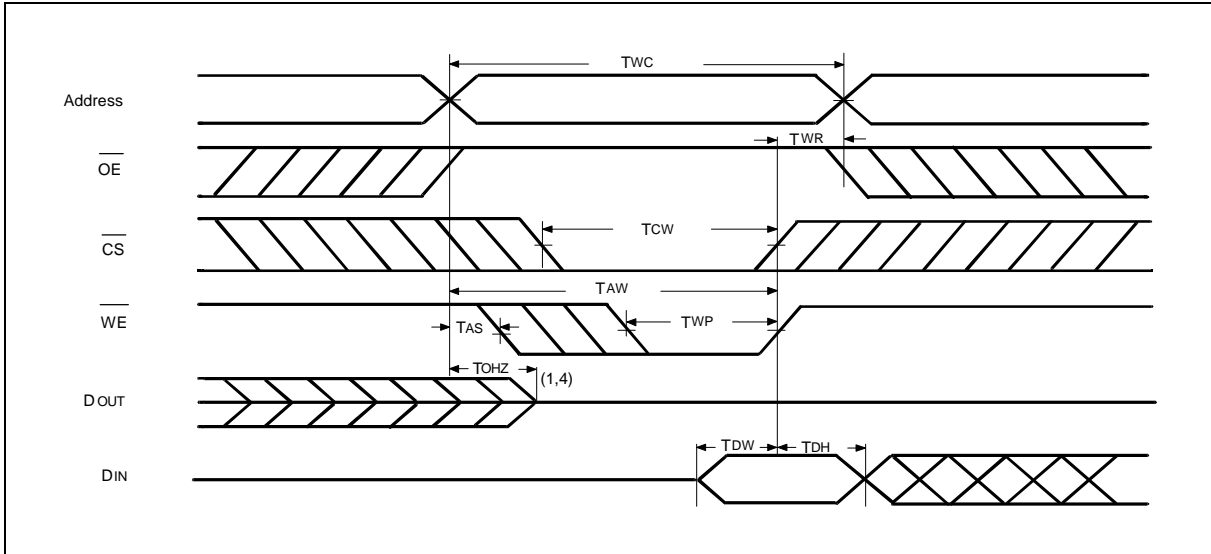




Timing Waveforms, continued

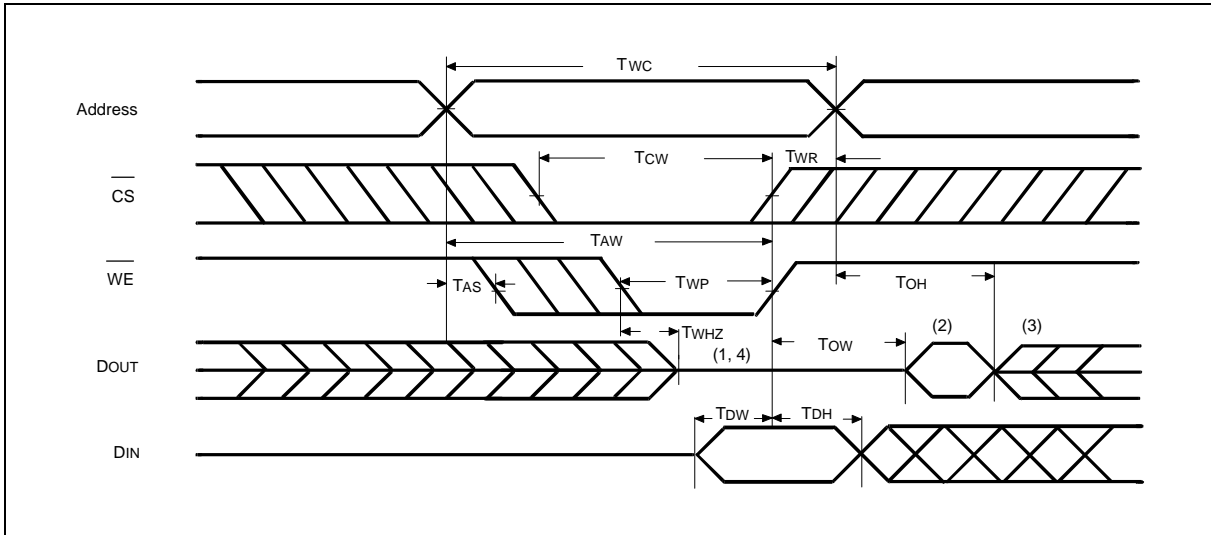
**Write Cycle 1**

( $\overline{OE}$  Clock)



**Write Cycle 2**

( $\overline{OE} = V_{IL}$  Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured  $\pm 500$  mV from steady state with  $C_L = 5$  pF. This parameter is guaranteed but not 100% tested.



## ORDERING INFORMATION

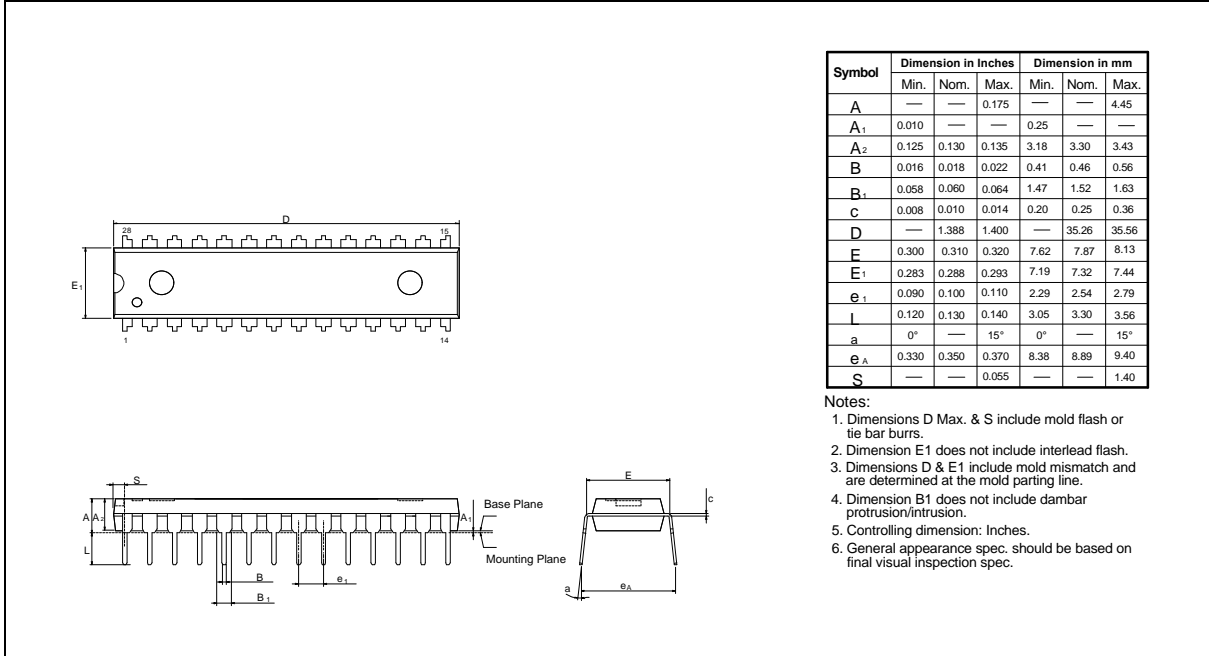
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (μA)	PACKAGE
W24L257AK-12	12	150	200	300 mil Skinny
W24L257AK-15	15	120	200	300 mil Skinny
W24L257AK-20	20	100	200	300 mil Skinny
W24L257AJ-12	12	150	200	300 mil SOJ
W24L257AJ-15	15	120	200	300 mil SOJ
W24L257AJ-20	20	100	200	300 mil SOJ
W24L257AQ-12	12	150	200	Standard type one TSOP
W24L257AQ-15	15	120	200	Standard type one TSOP
W24L257AQ-20	20	100	200	Standard type one TSOP

Notes:

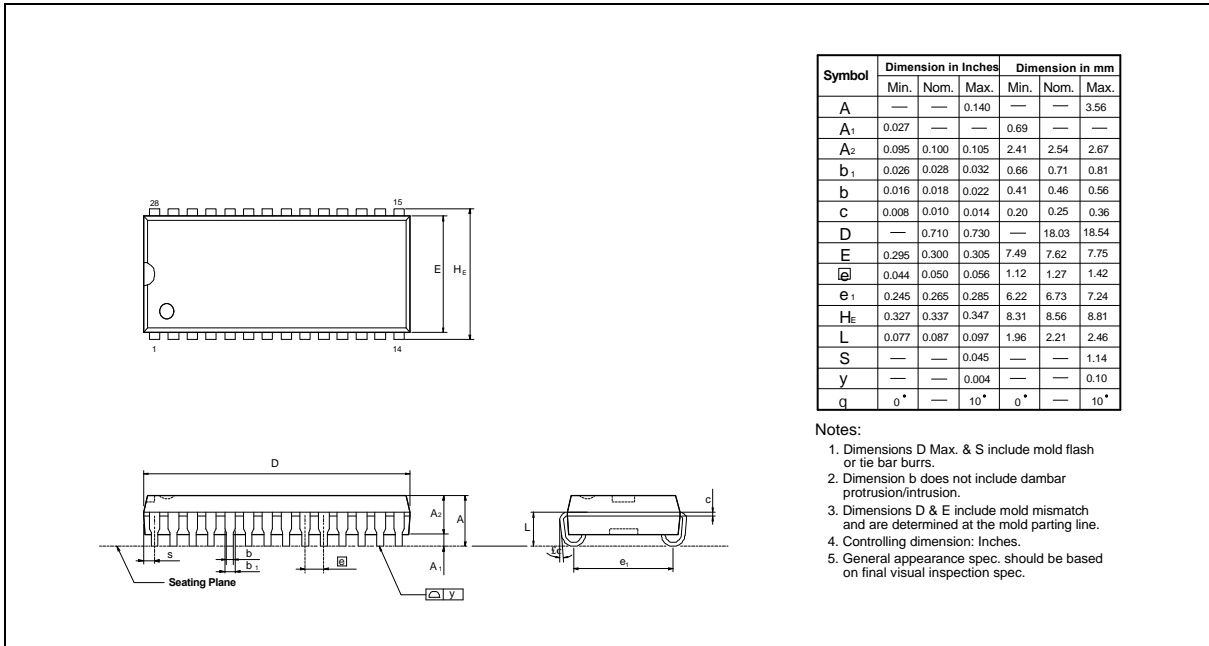
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

## PACKAGE DIMENSIONS

### 28-pin P-DIP Skinny



### 28-pin Small Outline J Band

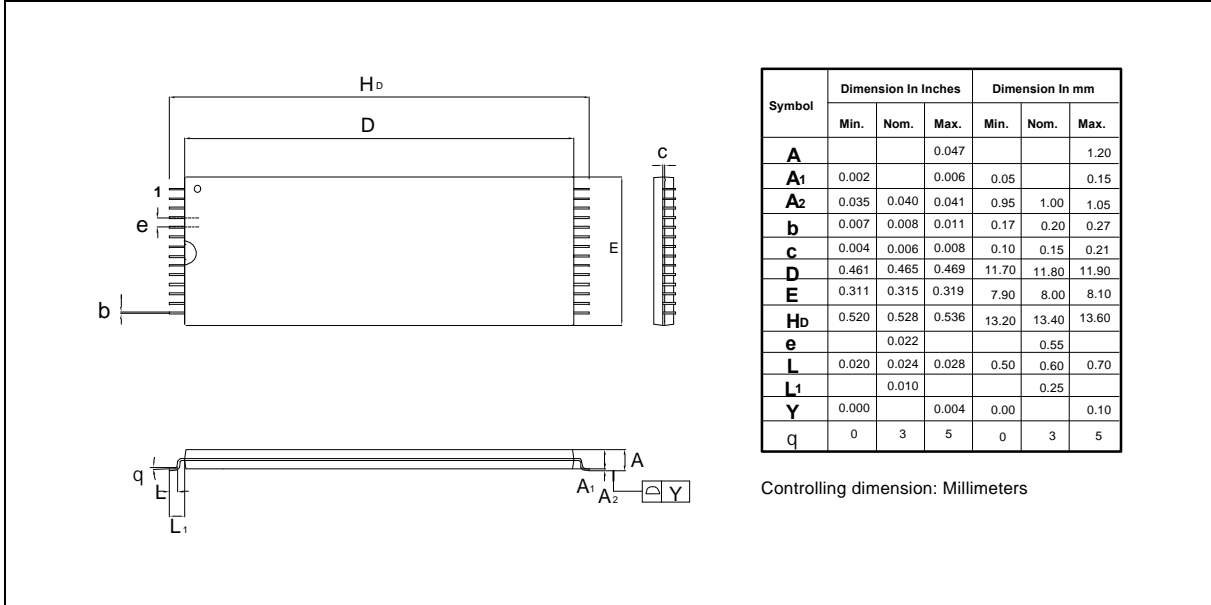






Package Dimensions, continued

## 28-pin Standard Type One TSOP



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Note: All data and specifications are subject to change without notice.