GENERAL DESCRIPTION

OB2298 is a highly integrated current mode PWM controller for medium to high power offline flyback converter applications.

OB2298 integrates PFC IC power supply control function and shuts down PFC stage at no load or light load conditions.

To meet the increasing stringent standby power requirements in light or zero load, OB2298 operates in On-Bright's proprietary "extended burst mode" without audio noise. Constant power limit is achieved by On-Bright's proprietary OCP compensation technique where OCP due to CCM and DCM mode difference is compensated in universal AC input applications.

OB2298 offers comprehensive protection coverage including Cycle-by-Cycle current limiting, internal Power-On Soft Start, VDD Under Voltage Lockout (UVLO), VDD Over Voltage Protection (OVP), VDD Clamp, Gate Clamp, Over Load Protection (OLP), Over Temperature Protection (OTP), Programmable Brownout Protection, All Pins Floating Protection, and RT Latch triggering feature.

In applications where VDD is supplied by auxiliary power supply, the built-in 1 second restart timer can prevent permanent OLP latch. In other applications, this restart timer will not be triggered.

To achieve good EMI performance, On-Bright's proprietary built-in frequency shuffling is provided, also with soft switching control at the totem pole gate drive output.

OB2298 is offered in SOP-8 and DIP-8 packages.

FEATURES

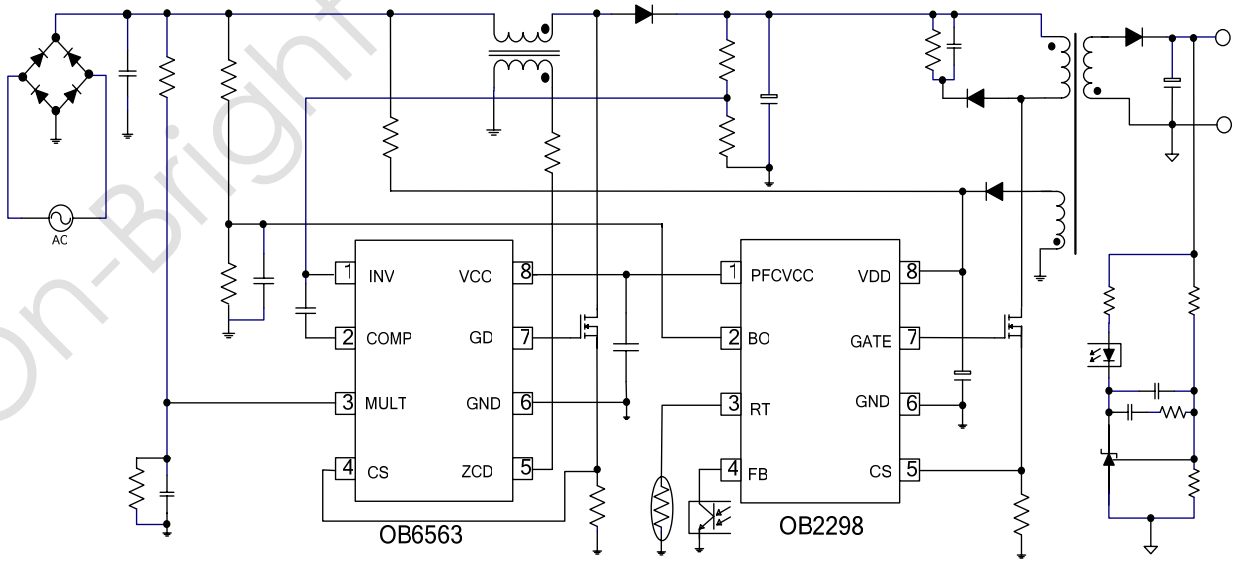
- Direct Control of PFC
- Programmable Brownout Protection
- Internal 4ms Power On Soft Start Time
- Internal Restart Timer
- Pin Floating Protection
- Proprietary Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Built-in Frequency Shuffling for Better EMI
- Built-in Leading Edge Blanking
- Proprietary OCP Compensation for Universal AC Input Range
- Low Startup Current(5uA) and Low Operating Current (2.3mA)
- Built-in Synchronized Slope Compensation
- 1.0A Peak Current Driving Capability
- Audio Noise Free Operation
- Convenient High and Low Triggering Level Latch Off Function

APPLICATIONS

Offline AC/DC flyback converter for

- Laptop Power Adaptor
- LCD Monitor Power
- LCD TV Power and Home Appliance Power
- Printer Power
- Lighting Power

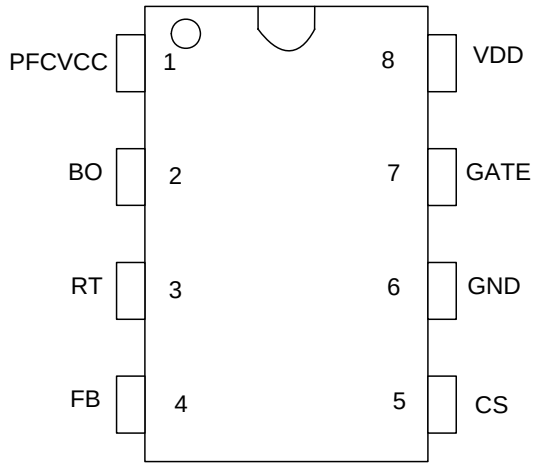
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The pin map of OB2298 in DIP8 and SOP8 package is shown as below.



Ordering Information

Part Number	Description
OB2298AP	DIP8, Pb-free
OB2298CP	SOP8, Pb-free
OB2298CPA	SOP8, Pb-free in Taping

.

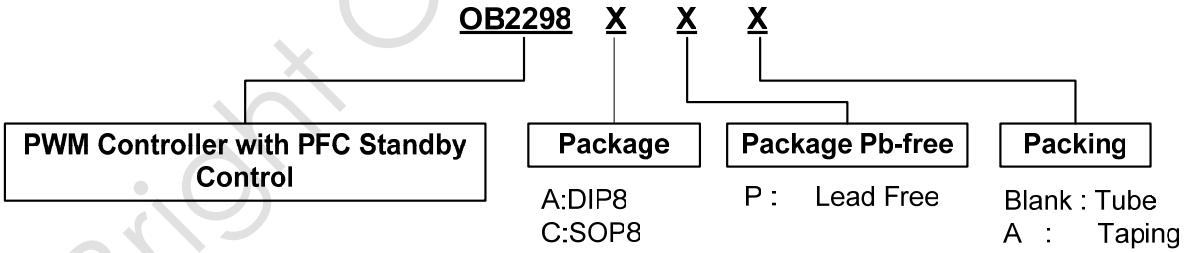
Package Dissipation Rating

Package	RθJA (°C/W)
DIP8	90
SOP8	150

Absolute Maximum Ratings

Parameter	Value
VDD Zener Clamp Voltage	30 V
VDD Clamp Continuous Current	10 mA
BO Input Voltage	-0.3 to 7V
RT Input Voltage	-0.3 to 7V
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-20 to 150 °C
Min/Max Storage Temperature T_{stg}	-55 to 150 °C
Lead Temperature (Soldering, 10secs)	260 °C

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



Marking Information

DIP

Y:Year Code(0-9)
WW:Week Code(01-52)
A:DIP8 Package
P:Pb-free Package
S:Internal Code(Optional)

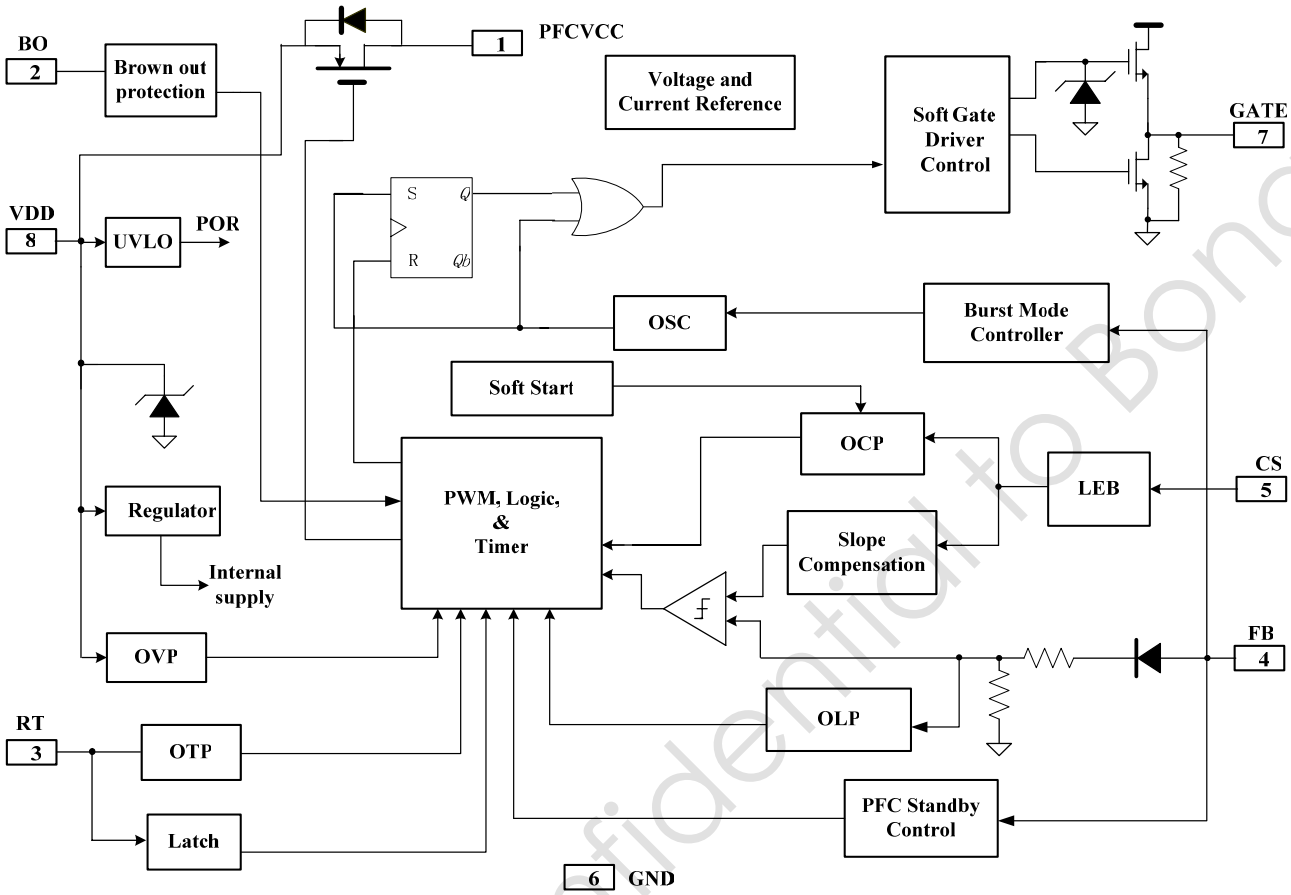
SOP

Y:Year Code(0-9)
WW:Week Code(01-52)
C:SOP8 Package
P:Pb-free Package
S:Internal Code(Optional)

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	PFCVCC	P	This pin is directly connected to the VDD pin (Pin 8) via a low impedance switch. During the startup sequence, the switch is off thus the power supply to PFC stage. As soon as the aux. winding is stabilized. The switch is on and provides power supply to the PFC controller. It goes down at No/Light load or fault conditions.
2	BO	I/O	Connected a resistor divider from line voltage to this pin to detect line voltage. If this pin drops below 1.05V and lasts 100ms, PWM output will be disabled. When brownout is triggered, this pin will disable an internal current for brownout hysteresis programming.
3	RT	I	Temperature sensing input pin. Connected to a NTC resistor to GND. Once the voltage of the RT pin drops below a fixed limit of 1.05V, PWM output will be disabled. When this pin is above 4.0V or below 0.6V, the PWM controller is latched shutdown.
4	FB	I	Feedback input pin. PWM duty cycle is determined by the voltage level into this pin and current sense signal level at Pin 5.
5	CS	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
6	GND	P	Ground
7	GATE	O	Totem-pole gate drive output for power MOSFET.
8	VDD	P	DC power supply pin.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min	Max	Unit
VDD	VDD Supply Voltage	12	25	V
T_A	Operating Ambient Temperature	-20	85	°C

ELECTRICAL CHARACTERISTICS

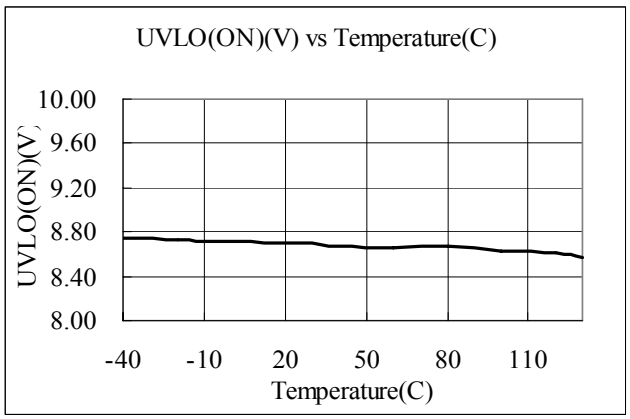
(T_A = 25^{O}C, VDD=18V, if not otherwise noted)

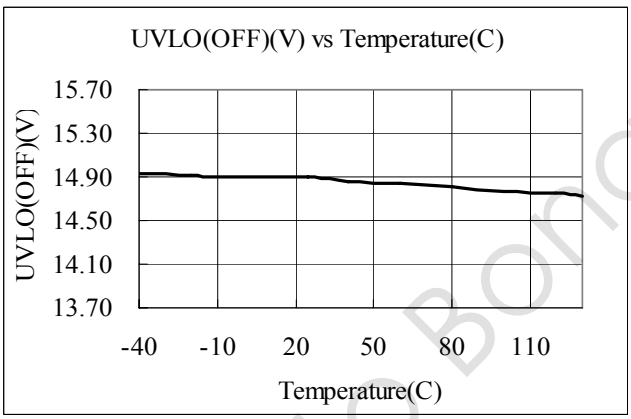
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD) Section						
Istartup	VDD start up current	VDD=14V, Measure current into VDD		5	20	uA
I_VDD	Operation current	V_{FB}=3V		2.3		mA
UVLO(ON)	VDD under voltage lockout enter		8	9	10	V
UVLO(OFF)	VDD under voltage lockout exit (Startup)		14.5	15.5	16.5	V
OVP(Latch)	VDD over voltage latch trigger		26	28	30	V
VDD(De-Latch)	VDD latch release threshold voltage			6.5		V
Ivdd_latch	VDD bleeding current at latch shutdown	VDD=8V		45		uA
T_D_OVP	VDD OVP Debounce time			100		uSec
V_{DD}_Clamp	V_{DD} zener clamp voltage	I(V_{DD}) = 10 mA		30		V
T_Softstart	Soft start time			4		mSec
Feedback Input Section(FB Pin)						
A_{VCS}	PWM input gain	V_{FB}/V_{cs}		2.4		V/V
V_{FB}_Open	FB open voltage			5.5		V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND, measure current		1.1		mA
V_{TH}_0D	Zero duty cycle FB threshold voltage				1	V
V_{TH}_GM	Green mode FB threshold voltage			1.7		V
V_{TH}_BM_on	Burst mode on FB threshold voltage			1.3		V
V_{TH}_BM_off	Burst mode off FB threshold voltage			1.4		V
V_{TH}_PL	Power limiting FB threshold voltage			4.4		V
T_D_PL	Power limiting debounce time			225		mSec
Z_{FB}_IN	Input impedance			5		Kohm
V_{TH}_PFC_off	PFC off FB threshold voltage			1.6		V
V_{TH}_PFC_on	PFC on FB threshold voltage			1.7		V
Current Sense Input(CS Pin) Section						
T_blanking	CS input leading edge blanking time			300		nSec
V_{TH}_OC	Internal current limiting threshold	Zero duty cycle	0.57	0.6	0.63	V

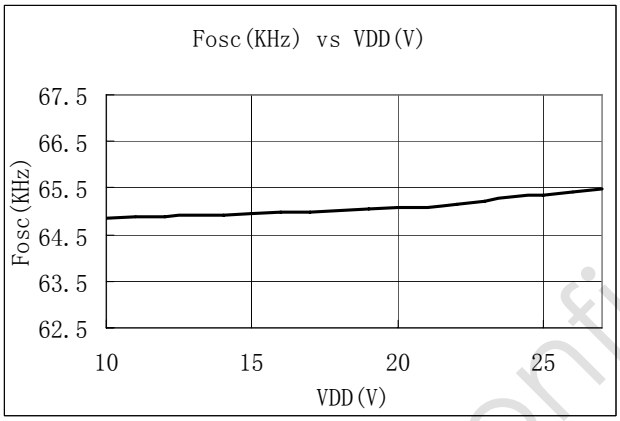
T_{D_OC}	Over current Detection to gate off delay time	CL=1nF at GATE,		100		nSec
Slope_Vth_oc	The slope that Vth_oc change with duty cycle	30% duty-cycle		0.63		V
Vpk_ocp	Maximum OCP threshold			0.80		V
Oscillator and Clock						
Fosc	Normal oscillation frequency	FB>1.7V	60	65	70	KHZ
	Frequency temperature stability	Temperature from -20℃ to 125℃		3		%
	Frequency voltage stability	VDD from 10V to 25V		3		%
Fosc_min	Mimimum oscillation frequency	FB<1.2V		22		KHZ
D_max	Maximum duty cycle			85		%
Frequency shuffling			-4		+4	%
Shuffling repetitivity				125		HZ
Gate Drive Output						
VOL	Output low level	Io = 30 mA (sink)			1	V
VOH	Output high level	Io = 30 mA (source)	7.5			V
VG_Clamp	Output clamp voltage level	VDD=25V		16		V
Tr_slow	Soft driver rising time	CL=1nF, Rising time from 0V to 6V		160		nSec
Tr_fast	Output rising time	CL = 1nF, Rising time from 6V to 13.5V		30		nSec
T_f	Output falling time	CL = 1nF, Falling time from 13.5V to 1.5V.		30		nSec
Over Temperature Protection						
I_RT	Output current of RT pin		95	100	105	uA
V_{TH_OTP}	OTP threshold voltage		1.0	1.05	1.1	V
$V_{TH\_RT\_latch1}$	RT input latch threshold voltage			0.6		V
$V_{TH\_RT\_latch2}$	RT input latch threshold voltage			4.0		V
T_{D_OTP}	OTP de-bounce time			100		uSec
V_RT_Open	RT pin open voltage			3.0		V
Brownout Section						
Vth_BO	Brownout comparator threshold voltage		1	1.05	1.1	V
T_{D_BO}	Brownout debounce time			100		ms
IBO_hys	BO output current for BO hysteresis programming			1.5		uA

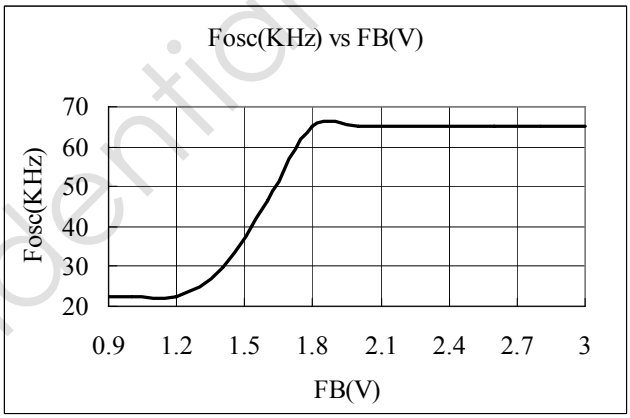
Restart Timer Section						
RST_auto	Auto recovery restart timer			1		Sec
PFCVCC section						
Rdson	Switch on resistor	Capable of delivering 40mA	10	20	30	Ω
Tpfc_off_delay	PFC go to standby debounce time			125		ms
Tpfc_on_delay	PFC on debounce time			10		mS

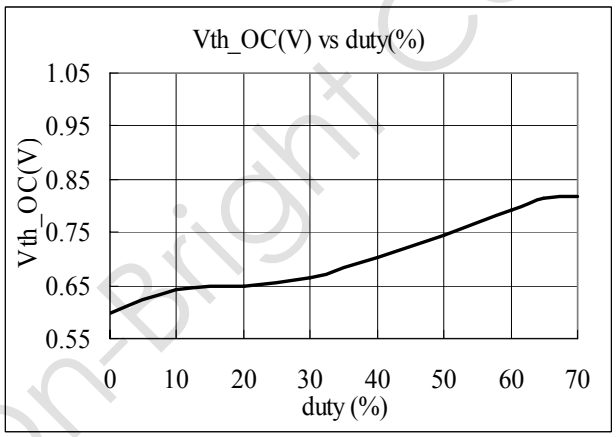
CHARACTERIZATION PLOTS

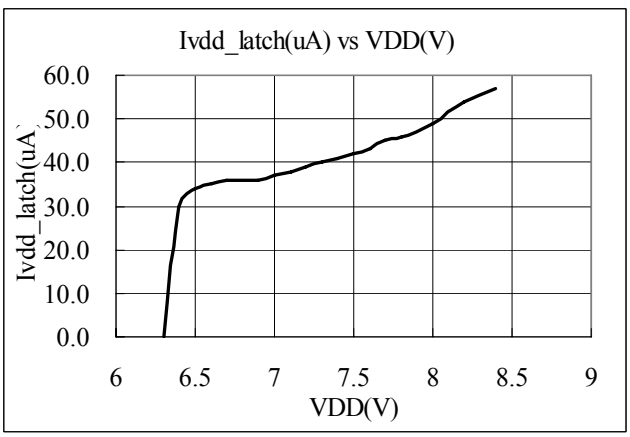


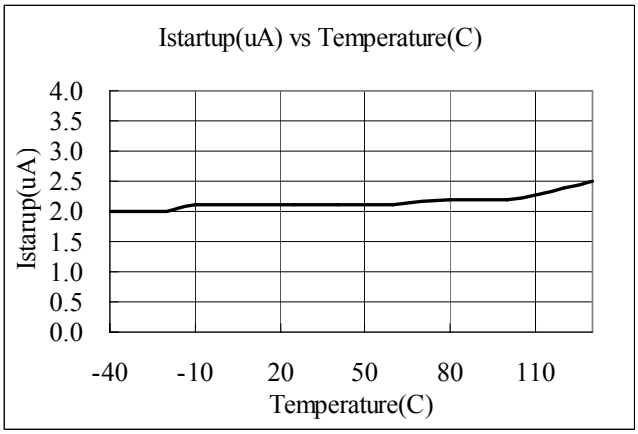


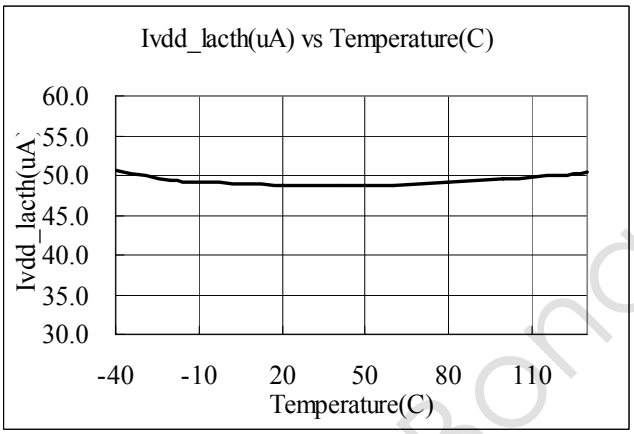


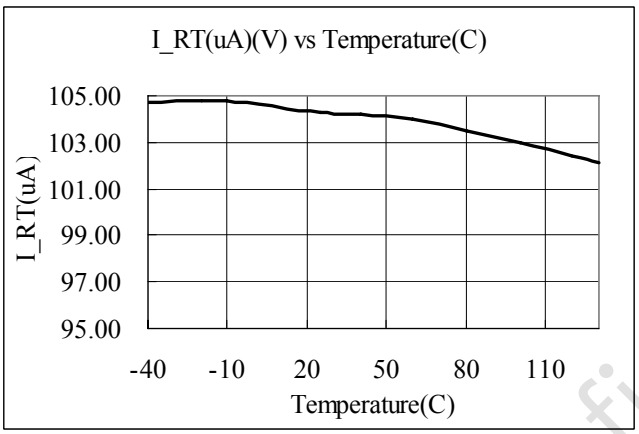


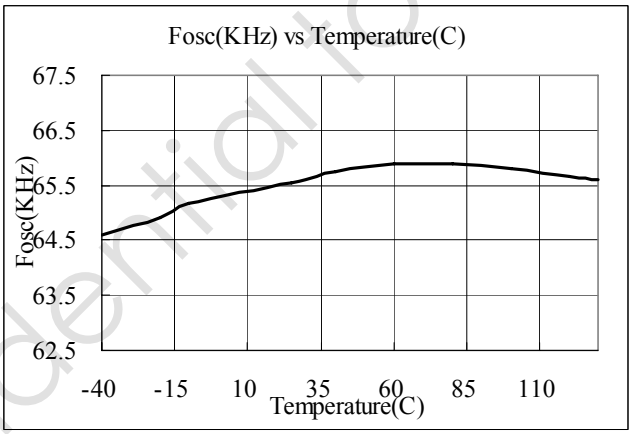


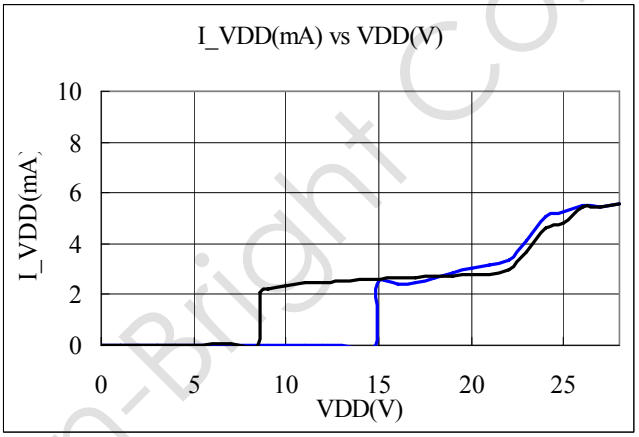












OPERATION DESCRIPTION

OB2298 integrates PFC IC power control functions to supply PFC IC power and shuts it down at No/Light load or any fault conditions. It is compatible with main stream PFC ICs in the market. The versatile protections and high performance make it very suitable for medium-to-large power applications.

- **PFCVCC Power On/off Control**

In applications with output power of greater than 75W, PFC pre-regulator is mandatory to meet the requirement of power factor, that is, a PFC pre-regulation is in the first stage and followed by a PWM controlled power conversion. However, this two-stage conversion makes it difficult to meet standby power requirement. To meet both requirements for power factor and standby, the PFC stage is off at No/Light conditions.

OB2298 provides the direct control for the operation of PFC stage. PFCVCC pin can be directly connected to PFC controller's power supply by a built-in low impedance power switch. In this way, PFC stage is controlled by PWM stage. OB2298 is compatible with main stream PFC ICs in the market. OB2298 shuts down the front end PFC stage at three situations: any fault occurs, No/Light load conditions and during start up sequence. Fig.1 illustrates a startup sequence and PFC On/off control at light loadings.

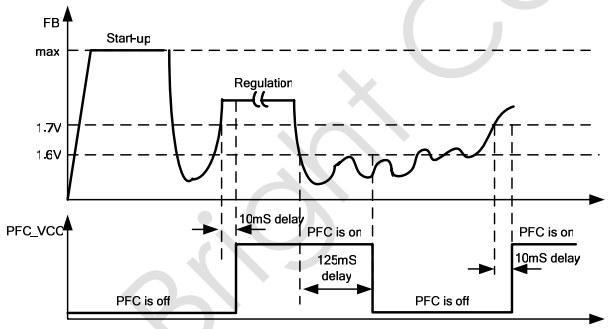


Figure 1

- **Startup Current and Start up Control**

Startup current of OB2298 is designed to be very low so that VDD could be charged up above UVLO(OFF) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC SMPS with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

- **Operating Current**

The Operating current of OB2298 is low at 2.3mA typically. Ultra low standby power is achieved with OB2298 low operating current together with extended burst mode control schemes.

- **Extended Burst Mode Operation**

At No load/Light load condition, most of the power dissipation in a SMPS is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. OB2298 self adjusts the switching mode according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level. Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss thus reduce the standby power consumption to the greatest extend. The nature of high frequency switching also reduces the audio noise at any loading conditions.

- **Oscillator/Frequency Shuffling Operation**

A fixed 65KHZ frequency oscillator is built in OB2298, and the proprietary frequency shuffling method can soften the EMI signature by spreading the energy in the vicinity of the main switching component. The magnitude of shuffling lies in the ranged of ±4% of the main switching frequency.

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in OB2298 current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filtering on sense input is no longer needed. The current limit comparator is disabled and cannot turn off the external MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

- **Internal Synchronized Slope Compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Over Temperature Protection (OTP)**

A NTC resistor in series with a regular resistor should connect between RT and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal current I_{RT} flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal OTP circuit is triggered and shutdown the MOSFET when the sensed input voltage is lower than V_{TH}_OTP. OTP is a latched shutdown.

- **RT Pin Used as Latch Shutdown Input Control**

RT pin could also be used as a control input to implement system latch shutdown function. An example is to implement system OVP protection with a latch shutdown function through a photo coupler and affiliated circuits. When OVP detection signal connected to RT is lower than 0.6V or higher than 4.0V, OB2298 controls system into latch shutdown. The recovery of the AC/DC conversion system could be only realized by resetting internal latch when VDD voltage drops below VDD(De-latch) value. This could be achieved by unplugging/re-plugging of AC source in AC start-up configuration.

- **Programmable Brownout Protection**

By monitoring the level on pin BO during normal operation, the controller protects the SMPS against low main condition. Fig.2 illustrates brownout protection implementation in OB2298. An internal 1.5uA current source is for brownout hysteresis window programming. The other 0.5uA source current is for BO pin floating protection. When BO level falls below 1.05V, the controller and lasts for about 100ms, the controller stops pulsing until this level goes back and resumes operation. By adjusting the resistor divider connected between the high input voltage and this pin, start and stop levels are programmable.

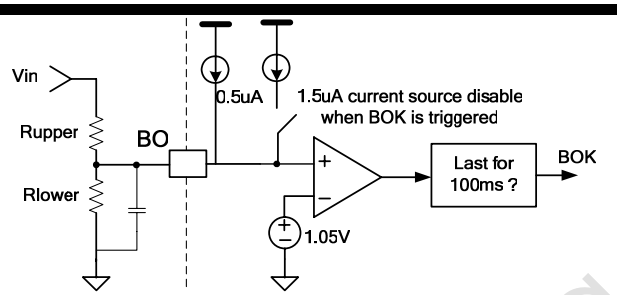


Figure 2

$$V_{BOP} = (\frac{1.05}{Rlower} - 2\times10^{-6}) \times Rupper + 1.05$$

$$V_{HYS} = 1.5\times10^{-6} \times Rupper$$

- **Over Load Protection (OLP)**

When over load (for example, short circuit) occurs, a fault is detected. If this fault is present for more than 225ms, OB2298 enters an auto-recovery soft burst mode. All pulses are stopped, VDD will drops below UVLO(ON) and the controller will try to restart, with the power on soft start. If the fault has gone, the SMPS resumes operation. If the fault is still there, the burst sequence starts again.

- **Restart Timer**

In some special applications, such as LCD TV, the PWM stage is supplied by auxiliary power converter. The typical configuration is shown in Fig.3.

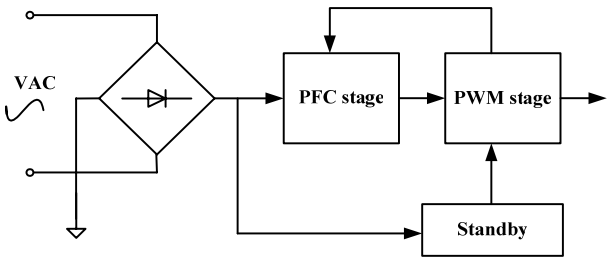


Figure 3

The front end is a PFC stage, followed by a PWM controlled power conversion stage. The PFC stage is controlled by PWM stage. At No/Light load, PWM shuts down PFC for better system power efficiency. However, the system needs a power source to monitor the whole system operation, this is done by a standby stage whose output provides the power supply to PWM stage. In situations of over loading (OLP), PWM stage enters the digital controlled latch mode and will not be auto-recovered since it is powered by standby stage. OB2298 will overcome this shortcoming by an internal restart timer. When OLP occurs, then the timer begins counting. When counting over, the OLP states will be cleared. If OLP still exists, then another counting cycle begins. The counting time in

OB2298 is 1 second. Therefore, the operation of OLP in the case of non-standby power stage is not disturbed.

- **Pin Floating Protection**

OB2298 provides all pin floating protection. In cases when the pins are floating, PWM switching is disabled, thus protect the power system.

- **Built-in Soft Start**

OB2298 features a built-in 4ms soft start to soften the constraints occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the peak current is gradually increased from nearly zero to the maximum clamping level 0.8V. The soft start is also activated during OLP sequence. Every restart attempt is followed by a soft start activation.

- **OCP compensation for CCM/DCM**

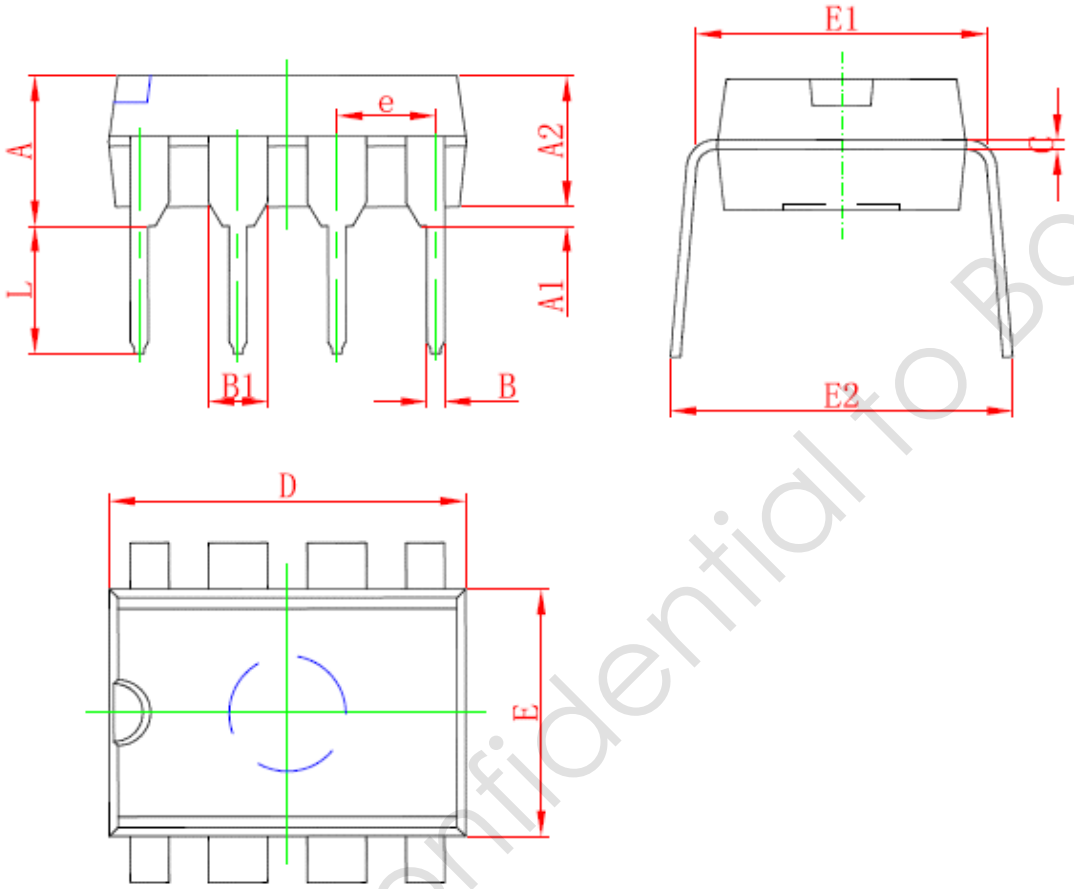
In OB2298, a proprietary OCP compensation is provided for better OCP performance in the universal input range. In conventional OCP compensation, only the gate delay is compensated. In OB2298, mode difference between CCM and DCM is also compensated, since in 90VAC the system often works in CCM. In this way, a more accurate OCP is achieved.

- **Gate Drive**

OB2298 Gate is connected to the Gate of an external MOSFET for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI. Good tradeoff is achieved through the built-in totem pole gate drive design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 16V clamp is added for MOSFET gate protection at higher than expected VDD input.

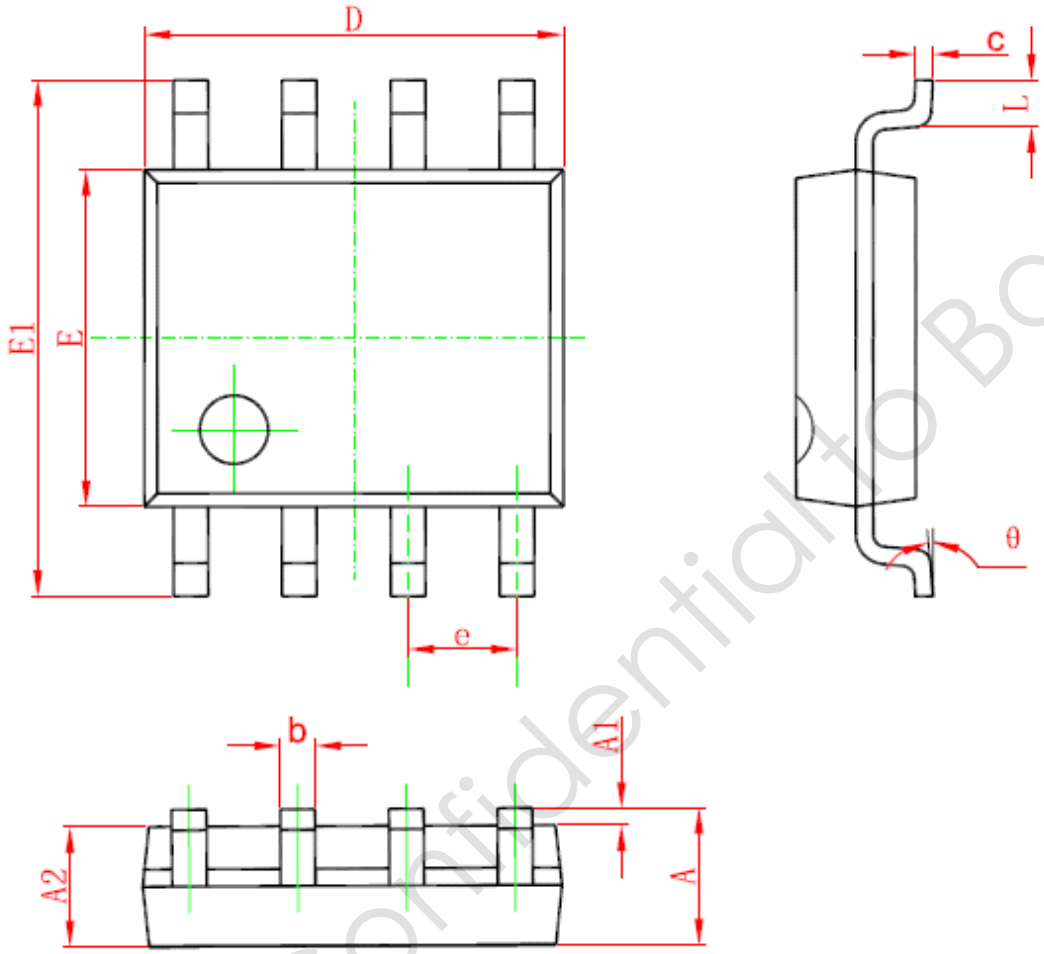
PACKAGE MECHANICAL DATA

8-Pin Plastic DIP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.500		0.020	
A2	3.200	3.600	0.126	0.142
B	0.350	0.650	0.014	0.026
B1	1.524 (BSC)		0.060 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	9.500	0.354	0.374
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.200	9.000	0.323	0.354

8-Pin Plastic SOP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.550	0.051	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0º	8º	0º	8º

IMPORTANT NOTICE

RIGHT TO MAKE CHANGES

On-Bright Electronics Corp. reserves the right to make corrections, modifications, enhancements, improvements and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

WARRANTY INFORMATION

On-Bright Electronics Corp. warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with its standard warranty. Testing and other quality control techniques are used to the extent it deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

On-Bright Electronics Corp. assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using On-Bright's components, data sheet and application notes. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

LIFE SUPPORT

On-Bright Electronics Corp.'s products are not designed to be used as components in devices intended to support or sustain human life. On-bright Electronics Corp. will not be held liable for any damages or claims resulting from the use of its products in medical applications.

MILITARY

On-Bright Electronics Corp.'s products are not designed for use in military applications. On-Bright Electronics Corp. will not be held liable for any damages or claims resulting from the use of its products in military applications.