



# BT169D

SCR

19 March 2014

Product data sheet

## 1. General description

Planar passivated Silicon Controlled Rectifier with sensitive gate in a SOT54 (TO-92) plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic ICs and other low power gate trigger circuits.

## 2. Features and benefits

- Planar passivated for voltage ruggedness and reliability
- Sensitive gate
- Direct triggering from low power gate circuits and logic ICs

## 3. Applications

- Ignition circuits
- Lighting ballasts
- Protection circuits
- Switched Mode Power Supplies

## 4. Quick reference data

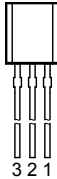

Table 1. Quick reference data

| Symbol                        | Parameter                            | Conditions   | Min | Typ | Max | Unit          |
|-------------------------------|--------------------------------------|--|-----|-----|-----|---------------|
| $V_{DRM}$                     | repetitive peak off-state voltage    |  | -   | -   | 400 | V             |
| $V_{RRM}$                     | repetitive peak reverse voltage      |  | -   | -   | 400 | V             |
| $I_{TSM}$                     | non-repetitive peak on-state current | half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a> | -   | -   | 8   | A             |
| $I_{T(AV)}$                   | average on-state current             | half sine wave; $T_{\text{lead}} \leq 83\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a>   | -   | -   | 0.5 | A             |
| $I_{T(RMS)}$                  | RMS on-state current                 | half sine wave; $T_{\text{lead}} \leq 83\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>                        | -   | -   | 0.8 | A             |
| <b>Static characteristics</b> |                                      |  |     |     |     |               |
| $I_{GT}$                      | gate trigger current                 | $V_D = 12\text{ V}$ ; $I_T = 10\text{ mA}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>                                   | -   | 50  | 200 | $\mu\text{A}$ |



## 5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline   | Graphic symbol  |
|-----|--------|-------------|--|---|
| 1   | A      | anode       |  <p>TO-92 (SOT54)</p> |  <p>A G K<br/>sym037</p> |
| 2   | G      | gate        |  |   |
| 3   | K      | cathode     |  |   |

## 6. Ordering information

Table 3. Ordering information

| Type number | Package |   |         |
|-------------|---------|---|---------|
|             | Name    | Description   | Version |
| BT169D      | TO-92   | plastic single-ended leaded (through hole) package; 3 leads | SOT54   |
| BT169D/01   | TO-92   | plastic single-ended leaded (through hole) package; 3 leads | SOT54   |
| BT169D/DG   | TO-92   | plastic single-ended leaded (through hole) package; 3 leads | SOT54   |

## 7. Marking

Table 4. Marking codes

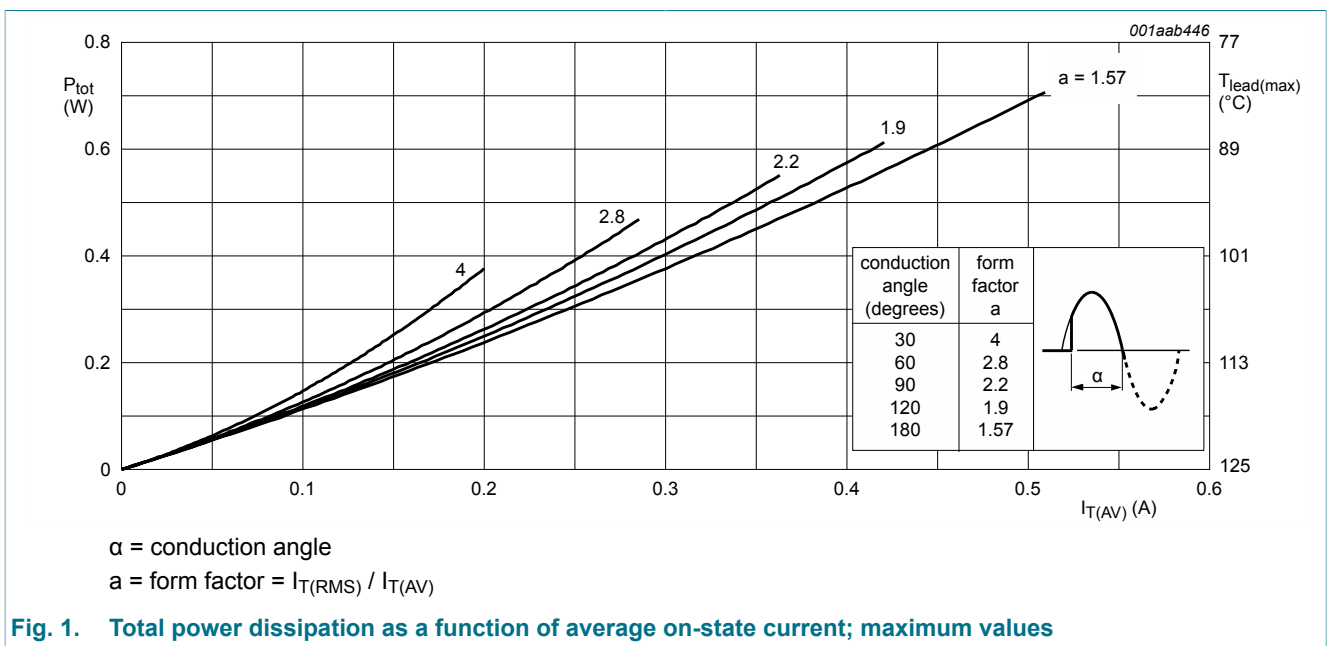
| Type number | Marking code |
|-------------|--------------|
| BT169D      | BT169DH      |
| BT169D/01   | BT169D       |
| BT169D/DG   | BT169DH      |

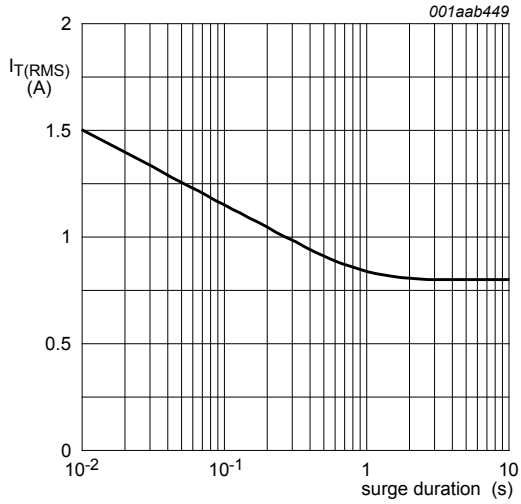
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

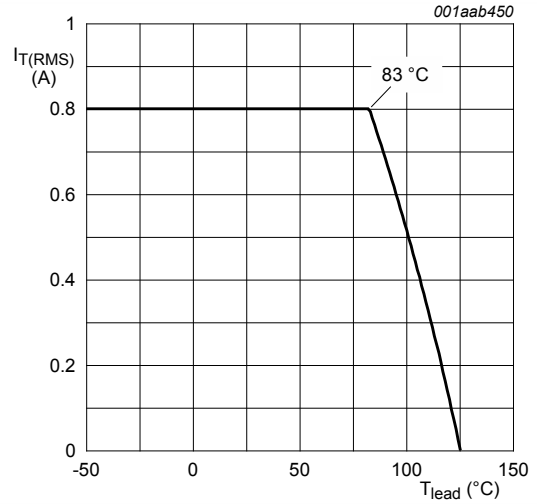
| Symbol       | Parameter                            | Conditions  | Min | Max  | Unit                   |
|--------------|--------------------------------------|---|-----|------|------------------------|
| $V_{DRM}$    | repetitive peak off-state voltage    |   | -   | 400  | V                      |
| $V_{RRM}$    | repetitive peak reverse voltage      |   | -   | 400  | V                      |
| $I_{T(AV)}$  | average on-state current             | half sine wave; $T_{lead} \leq 83\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a>   | -   | 0.5  | A                      |
| $I_{T(RMS)}$ | RMS on-state current                 | half sine wave; $T_{lead} \leq 83\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>                        | -   | 0.8  | A                      |
| $I_{TSM}$    | non-repetitive peak on-state current | half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a> | -   | 8    | A                      |
|              |                                      | half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 8.3\text{ ms}$  | -   | 9    | A                      |
| $I^2t$       | $I^2t$ for fusing                    | $t_p = 10\text{ ms}$ ; SIN  | -   | 0.32 | $\text{A}^2\text{s}$   |
| $dl_T/dt$    | rate of rise of on-state current     | $I_T = 2\text{ A}$ ; $I_G = 10\text{ mA}$ ; $dl_G/dt = 100\text{ mA}/\mu\text{s}$   | -   | 50   | $\text{A}/\mu\text{s}$ |
| $I_{GM}$     | peak gate current                    |   | -   | 1    | A                      |
| $V_{RGM}$    | peak reverse gate voltage            |   | -   | 5    | V                      |
| $P_{GM}$     | peak gate power                      |   | -   | 2    | W                      |
| $P_{G(AV)}$  | average gate power                   | over any 20 ms period   | -   | 0.1  | W                      |
| $T_{stg}$    | storage temperature                  |   | -40 | 150  | $^{\circ}\text{C}$     |
| $T_j$        | junction temperature                 |   | -   | 125  | $^{\circ}\text{C}$     |



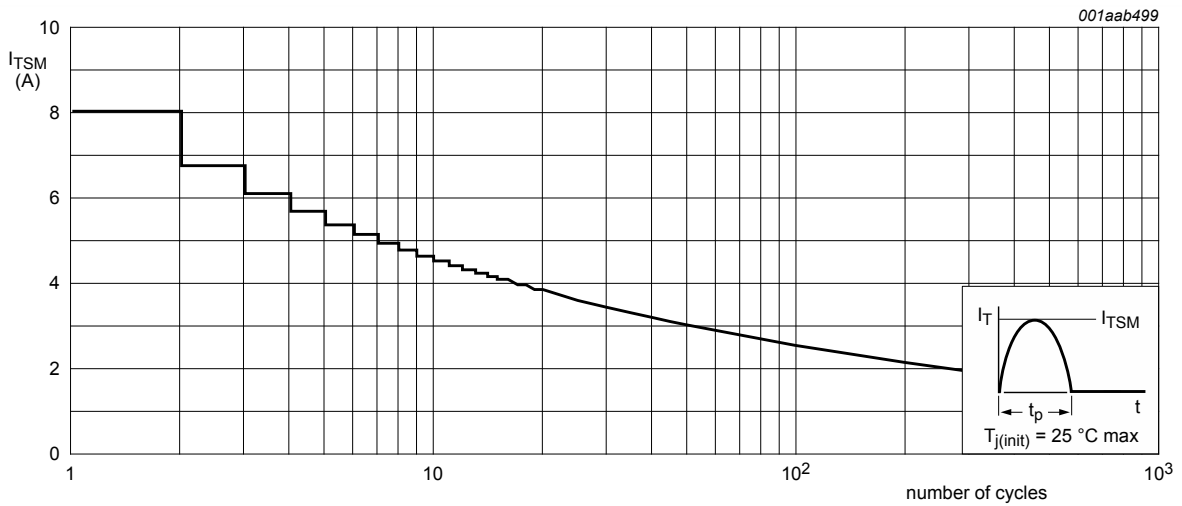


$f = 50 \text{ Hz}; T_{\text{lead}} = 83 \text{ }^\circ\text{C}$

**Fig. 2. RMS on-state current as a function of surge duration for sinusoidal currents**

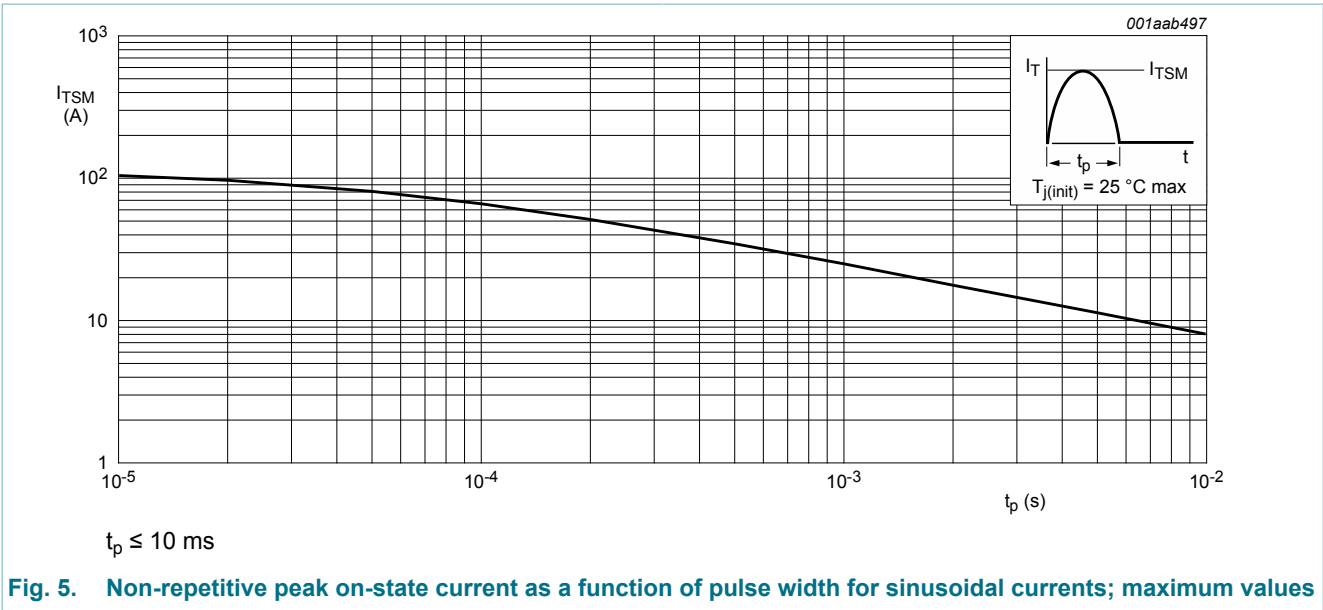


**Fig. 3. RMS on-state current as a function of lead temperature; maximum values**



$f = 50 \text{ Hz}$

**Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**



## 9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol           | Parameter                                   | Conditions  | Min | Typ | Max | Unit |
|------------------|---|---|-----|-----|-----|------|
| $R_{th(j-lead)}$ | thermal resistance from junction to lead    | <a href="#">Fig. 6</a>                            | -   | -   | 60  | K/W  |
| $R_{th(j-a)}$    | thermal resistance from junction to ambient | printed circuit board mounted: lead length = 4 mm | -   | 150 | -   | K/W  |

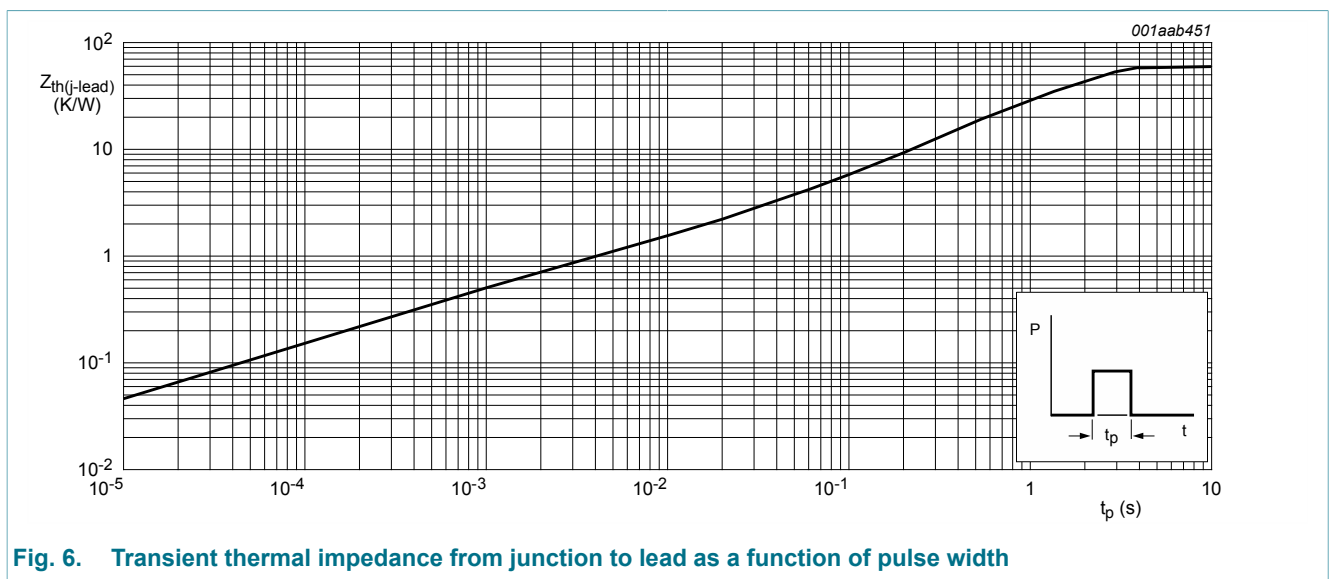
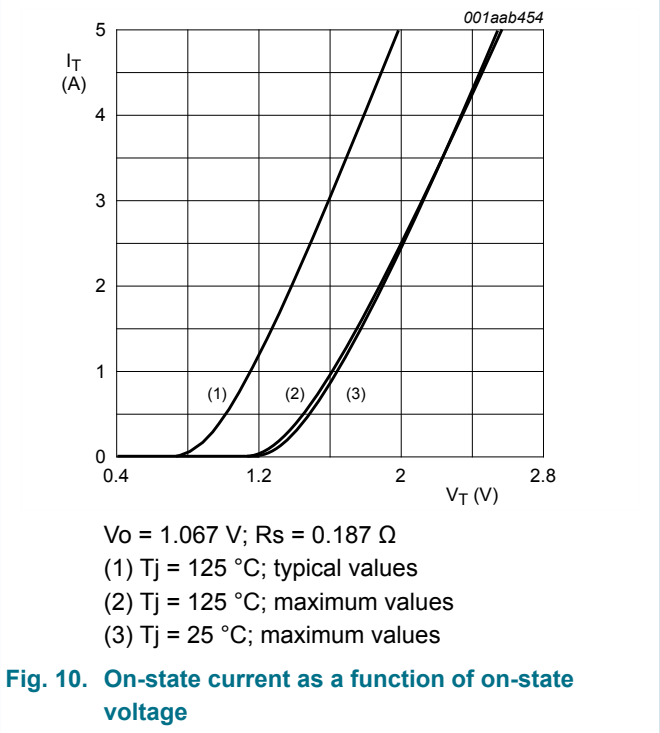
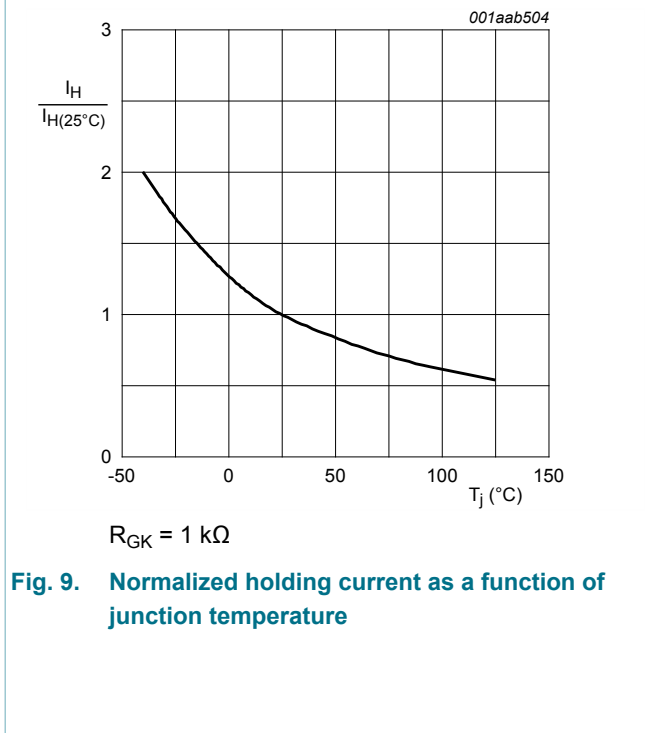
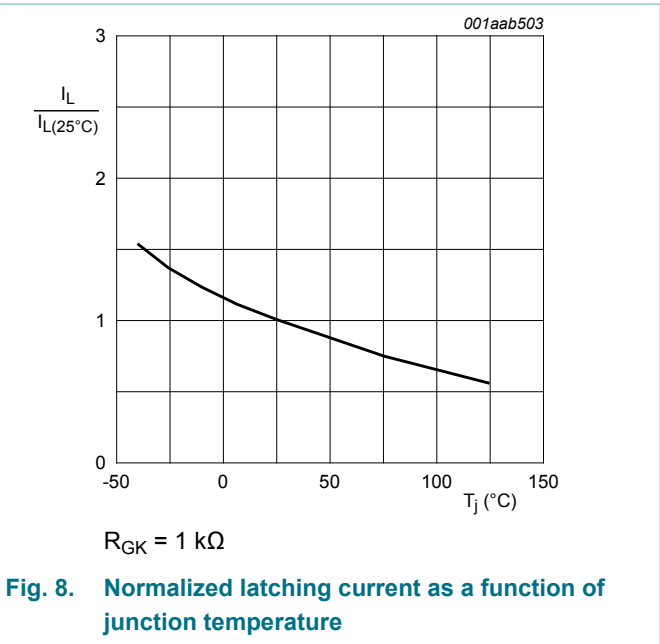
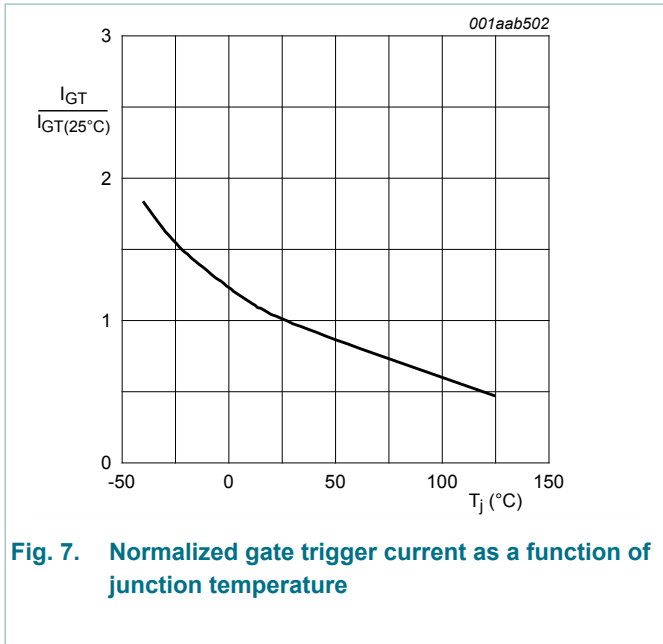


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

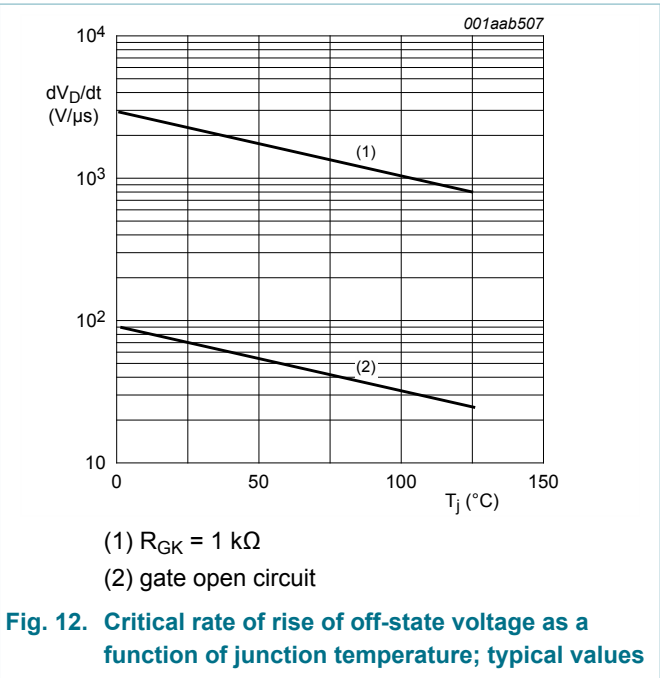
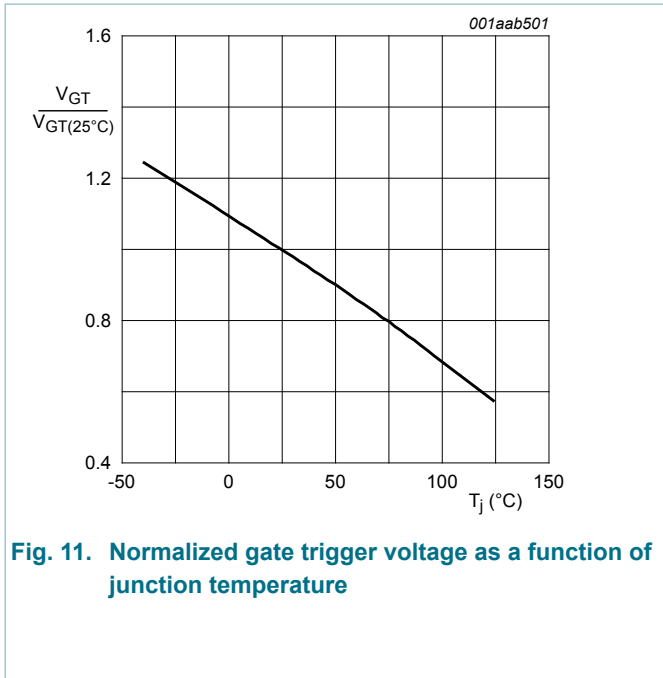
## 10. Characteristics

Table 7. Characteristics

| Symbol                         | Parameter                         | Conditions  | Min | Typ  | Max | Unit                   |
|--------------------------------|-----------------------------------|---|-----|------|-----|------------------------|
| <b>Static characteristics</b>  |                                   |   |     |      |     |                        |
| $I_{GT}$                       | gate trigger current              | $V_D = 12\text{ V}$ ; $I_T = 10\text{ mA}$ ; $T_j = 25\text{ }^\circ\text{C}$ ;<br><a href="#">Fig. 7</a>   | -   | 50   | 200 | $\mu\text{A}$          |
| $I_L$                          | latching current                  | $V_D = 12\text{ V}$ ; $I_G = 0.5\text{ mA}$ ; $T_j = 25\text{ }^\circ\text{C}$ ;<br><a href="#">Fig. 8</a>  | -   | 2    | 6   | mA                     |
| $I_H$                          | holding current                   | $V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>   | -   | 2    | 5   | mA                     |
| $V_T$                          | on-state voltage                  | $I_T = 1.2\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>   | -   | 1.25 | 1.7 | V                      |
| $V_{GT}$                       | gate trigger voltage              | $V_D = 12\text{ V}$ ; $I_T = 10\text{ mA}$ ; $T_j = 25\text{ }^\circ\text{C}$ ;<br><a href="#">Fig. 11</a>  | -   | 0.5  | 0.8 | V                      |
|                                |                                   | $V_D = 400\text{ V}$ ; $I_T = 10\text{ mA}$ ; $T_j = 125\text{ }^\circ\text{C}$ ;<br><a href="#">Fig. 11</a>  | 0.2 | 0.3  | -   | V                      |
| $I_D$                          | off-state current                 | $V_D = 400\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$  | -   | 0.05 | 0.1 | mA                     |
| $I_R$                          | reverse current                   | $V_R = 400\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$  | -   | 0.05 | 0.1 | mA                     |
| <b>Dynamic characteristics</b> |                                   |   |     |      |     |                        |
| $dV_D/dt$                      | rate of rise of off-state voltage | $V_{DM} = 268\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; $R_{GK} = 1\text{ k}\Omega$ ;<br>exponential waveform; <a href="#">Fig. 12</a>  | 500 | 800  | -   | $\text{V}/\mu\text{s}$ |
|                                |                                   | $V_{DM} = 268\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; exponential<br>waveform; gate open circuit; <a href="#">Fig. 12</a>   | -   | 25   | -   | $\text{V}/\mu\text{s}$ |
| $t_{gt}$                       | gate-controlled turn-on time      | $I_{TM} = 2\text{ A}$ ; $V_D = 400\text{ V}$ ; $I_G = 10\text{ mA}$ ; $dI_G/dt = 0.1\text{ A}/\mu\text{s}$ ; $T_j = 25\text{ }^\circ\text{C}$   | -   | 2    | -   | $\mu\text{s}$          |
| $t_q$                          | commutated turn-off time          | $V_{DM} = 268\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; $I_{TM} = 1.6\text{ A}$ ;<br>$V_R = 35\text{ V}$ ; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$ ; $dV_D/dt = 2\text{ V}/\mu\text{s}$ ; $R_{GK} = 1\text{ k}\Omega$ | -   | 100  | -   | $\mu\text{s}$          |







### 11. Package outline

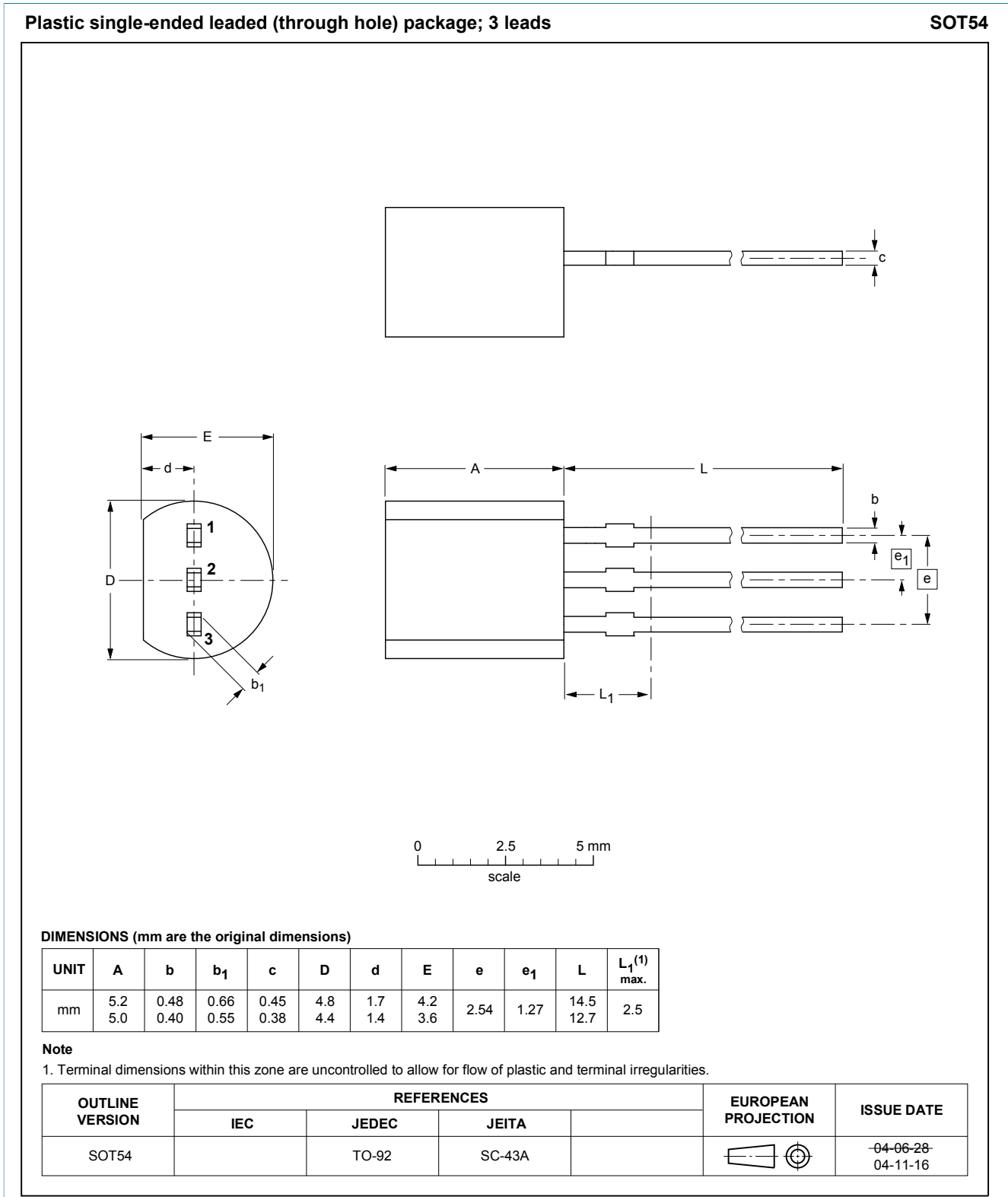


Fig. 13. Package outline TO-92 (SOT54)

## 12. Legal information

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|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
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