HM53461 Series, HM53462 Series

65,536-word × 4-bit Multiport CMOS Video RAM

The HM53461/HM53462 is a 262,144-bit multiport memory equipped with a 64 k-word × 4-bit dynamic RAM port and a 256-word × 4-bit serial access memory (SAM) port. The SAM port is connected to an internal 1,024-bit data register through a 256-word × 4-bit serial read or write access control. In the read transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of four data bits can be achieved. The Hitachi 2 µm CMOS process achieves a fast serial access operation and low power dissipation. All inputs and outputs, including clocks, are TTL compatible. In HM53462, the RAM port has logic operation capability. By using this function, logic operation between memory data and input data can be done in one cycle.

Features

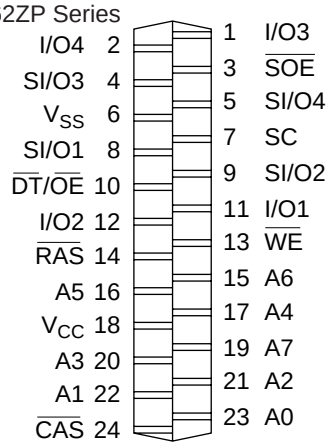
- Multiport organization
  (RAM; 64 k-word × 4-bit and SAM;
  256 word × 4-bit)
- Double layer polysilicon/polycide n-well CMOS process
- Single 5 V (±10%)
- Low power
  - — Active: RAM: 380 mW max
    SAM: 220 mW max
  - — Standby: 40 mW max.
- Access Time
  - — RAM: 100 ns/120 ns/150 ns
  - — SAM: 40 ns/40 ns/60 ns
- Cycle time
  - — Random read or write cycle time (RAM):
    190 ns/220 ns/260 ns
  - — Serial read or write cycle time (SAM):
    40 ns/40 ns/60 ns
- TTL compatible
- 256 refresh cycles: 4 ms
- Refresh function
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
- Data transfer operation (between RAM and SAM)
- Fast serial access operation asynchronized with RAM port (except data transfer cycle)
- Real time read transfer capability
- Write mask mode capability
- Logic operation capability between Din and Dout (HM53462 Series)
- SAM organization can be changed to 1024 × 1 (HM53462 Series)

Ordering Information

Type No.	Access Time	Package
HM53461P-10	100 ns	400-mil, 24-pin plastic DIP (DP-24A)
HM53461P-12	120 ns	
HM53461P-15	150 ns	
HM53461ZP-10	100 ns	24-pin plastic ZIP (ZP-24)
HM53461ZP-12	120 ns	
HM53461ZP-15	150 ns	
HM53461JP-10	100 ns	24-pin plastic SOJ (CP-24D)
HM53461JP-12	120 ns	
HM53461JP-15	150 ns	
HM53462P-10	100 ns	400-mil, 24-pin plastic DIP (DP-24A)
HM53462P-12	120 ns	
HM53462P-15	150 ns	
HM53462ZP-10	100 ns	28-pin plastic ZIP (ZP-24)
HM53462ZP-12	120 ns	
HM53462ZP-15	150 ns	
HM53462JP-10	100 ns	300-mil, 24-pin plastic SOJ (CP-24D)
HM53462JP-12	120 ns	
HM53462JP-15	150 ns	

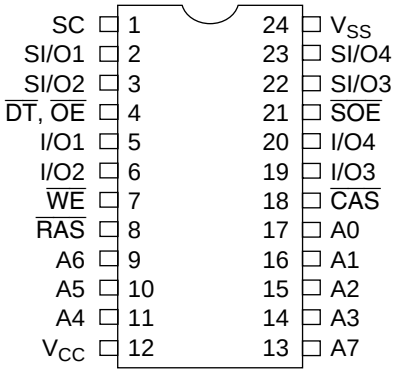
Pin Arrangement

HM53461ZP Series
HM53462ZP Series



(Bottom view)

HM53461P/JP Series
HM53462P/JP Series

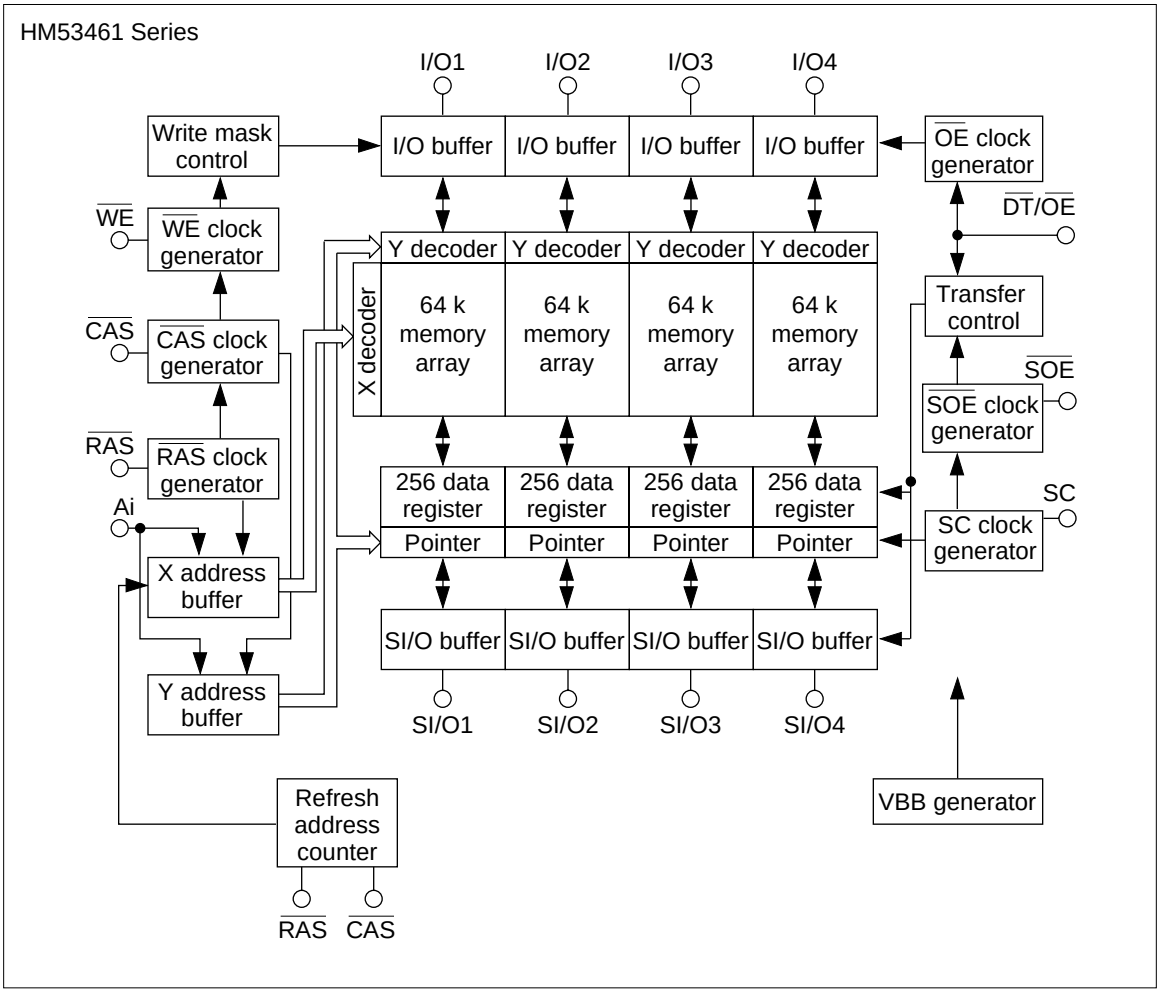


(Top view)

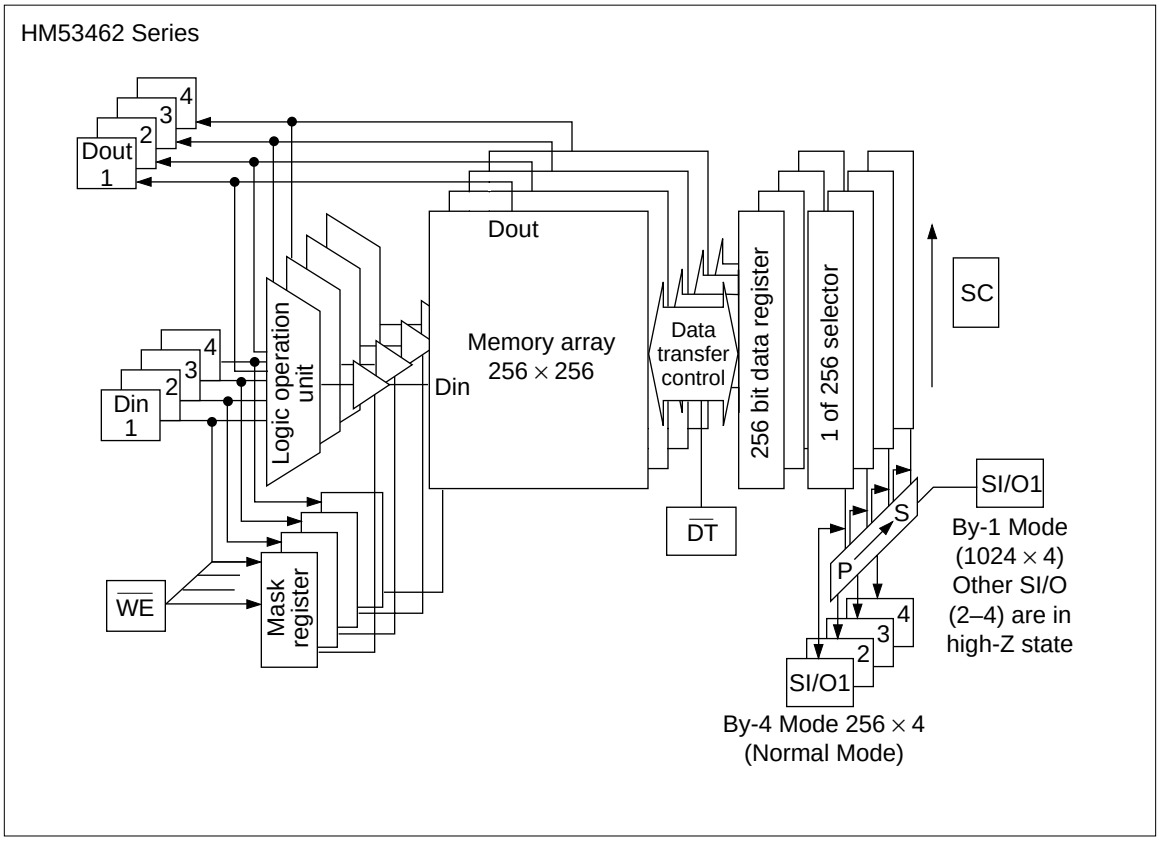
Pin Description

Pin Name	Function
A0–A7	Address inputs
I/O1–I/O4	RAM port data input/output
SI/O1–SI/O4	SAM port data input/output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
SC	Serial clock
$\overline{WE}$	Write enable
$\overline{DT}/\overline{OE}$	Data transfer/output enable
$\overline{SOE}$	SAM port enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Block Diagram (cont)



Absolute Maximum Ratings

- Voltage on any pin relative to V_{SS}: –1 V to +7 V
- Power supply voltage relative to V_{SS}: –0.5 V to +7 V
- Operating temperature, Ta (Ambient): 0°C to +70°C
- Storage temperature: –55°C to +125°C
- Short circuit output current: 50 mA
- Power dissipation: 1 W

Recommended DC Operating Conditions (Ta = 0 to +70°C)*1

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	6.0	V
Input low voltage	V_{IL}	–0.5 *2	—	0.8	V

Notes: 1. All voltages refernced to V_{SS}.
2. –3.0 V for pulse wideth ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

RAM port	Symbol	SAM port Standby	SAM port Active	HM53461-10 HM53462-10	HM53461-12 HM53462-12	HM53461-15 HM53462-15	Unit
Operating current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC1}	O	X	70	60	50	mA
	I_{CC7}	X	O	110	100	80	mA
Standby current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	I_{CC2}	O	X	7	7	7	mA
	I_{CC8}	X	O	40	40	30	mA
$\overline{RAS}$ only refresh current, $\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling, t_{RC} = min.	I_{CC3}	O	X	60	50	40	mA
	I_{CC9}	X	O	100	90	70	mA
Page mode current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min.	I_{CC4}	O	X	50	40	35	mA
	I_{CC10}	X	O	90	80	65	mA
CBR refresh current $\overline{RAS}$ cycling t_{RC} = min.	I_{CC5}	O	X	60	50	40	mA
	I_{CC11}	X	O	100	90	70	mA
Data transfer current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC6}	O	X	75	65	55	mA
	I_{CC12}	X	O	115	105	85	mA

Parameter	Symbol	Min	Max	Unit
Input leakage	I_{LI}	–10	10	µA
Output leakage	I_{LO}	–10	10	µA
Output high voltage I_{OH} = –2 mA	V_{OH}	2.4	—	V
Output low voltage I_{OL}= 4.2 mA	V_{OL}	—	0.4	V

Input/Output Capacitance

Parameter	Symbol	Typ	Max	Unit
Address	CI_1	—	5	pF
Clocks	CI_2	—	5	pF
I/O, SI/O	$C_{I/O}$	—	7	pF

Electrical Characteristics and Recommended AC Operating Conditions (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)[*1, 10, 11]

		HM53461-10 HM53462-10		HM53461-12 HM53462-12		HM53461-15 HM53462-15			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Note
Random read or write cycle time	t_{RC}	190	—	220		260	—	ns	
Read-modify-write cycle time	t_{RWC}	260	—	300	—	355	—	ns	
Page mode cycle time	t_{PC}	70	—	85	—	105	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	50	—	60	—	75	ns	3, 4
Output buffer turn off delay referenced to $\overline{CAS}$	t_{OFF1}	—	25	—	30	—	40	ns	5
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ precharge time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{RAS}$ hold time	t_{RSH}	50	—	60	—	75	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	

Electrical Characteristics and Recommended AC Operating Conditions (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)[*1, 10, 11] (cont)

		HM53461-10 HM53462-10		HM53461-12 HM53462-12		HM53461-15 HM53462-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	15	—	15	—	20	—	ns	
Column address setup time	t_{ASC}	0		0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	20	—	25	—	ns	
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	8
Write command hold time	t_{WCH}	25	—	25	—	30	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	35	—	40	—	45	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	35	—	40	—	45	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in hold time	t_{DH}	25	—	25	—	30	—	ns	8, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh period	t_{REF}	—	4	—	4	—	4	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	170	10000	200	10000	245	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	85	—	100	—	125	—	ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	—	25	—	30	—	ns	

Electrical Characteristics and Recommended AC Operating Conditions (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)[*1, 10, 11] (cont)

Parameter	Symbol	HM53461-10 HM53462-10 Min	HM53461-10 HM53462-10 Max	HM53461-12 HM53462-12 Min	HM53461-12 HM53462-12 Max	HM53461-15 HM53462-15 Min	HM53461-15 HM53462-15 Max	Unit	Note
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	15	—	20	—	ns	
Access time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	25	—	30	—	40	ns	
$\overline{OE}$ to data-in delay time	t_{ODD}	25	—	30	—	40	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	ns	
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{OE}$ to $\overline{RAS}$ delay time	t_{ORD}	35	—	40	—	45	—	ns	
Serial clock cycle time	t_{SCC}	40	—	40	—	60	—	ns	
Access time from SC	t_{SCA}	—	40	—	40	—	60	ns	10
Access time from $\overline{SOE}$	t_{SEA}	—	25	—	30	—	40	ns	10
SC pulse width	t_{SC}	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Serial data-out hold time after SC high	t_{SOH}	10	—	10	—	10	—	ns	
Serial output buffer turn off delay from $\overline{SOE}$	t_{SEZ}	—	25	—	25	—	30	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	25	—	ns	
$\overline{DT}$ to $\overline{RAS}$ setup tune	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time (read transfer cycle)	t_{RDH}	80	—	90	—	110	—	ns	

Electrical Characteristics and Recommended AC Operating Conditions (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)[*1, 10, 11] (cont)

Parameter	Symbol	HM53461-10 HM53462-10		HM53461-12 HM53462-12		HM53461-15 HM53462-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	15	—	15	—	20	—	ns	
$\overline{DT}$ to $\overline{CAS}$ hold time	t_{CDH}	20	—	30	—	45	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	10	—	ns	
First SC to $\overline{DT}$ hold time	t_{SDH}	25	—	25	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DTR}	10	—	10	—	10	—	ns	
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	20	—	ns	
I/O to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
I/O to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	20	—	ns	
Serial output buffer turn off delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	30	—	40	—	45	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	25	—	30	—	35	—	ns	
Serial data input delay time from $\overline{RAS}$	t_{SID}	50	—	60	—	75	—	ns	
Serial data input to $\overline{DT}$ delay time	t_{SZD}	0	—	0	—	0	—	ns	
$\overline{SOE}$ to $\overline{RAS}$ setup time	t_{ES}	0	—	0	—	0	—	ns	
$\overline{SOE}$ to $\overline{RAS}$ hold time	t_{EH}	15	—	15	—	20	—	ns	
Serial write enable setup time	t_{SWS}	0	—	0	—	0	—	ns	
Serial write enable hold time	t_{SWH}	35	—	35	—	55	—	ns	
Serial write disable setup time	t_{SWIS}	0	—	0	—	0	—	ns	

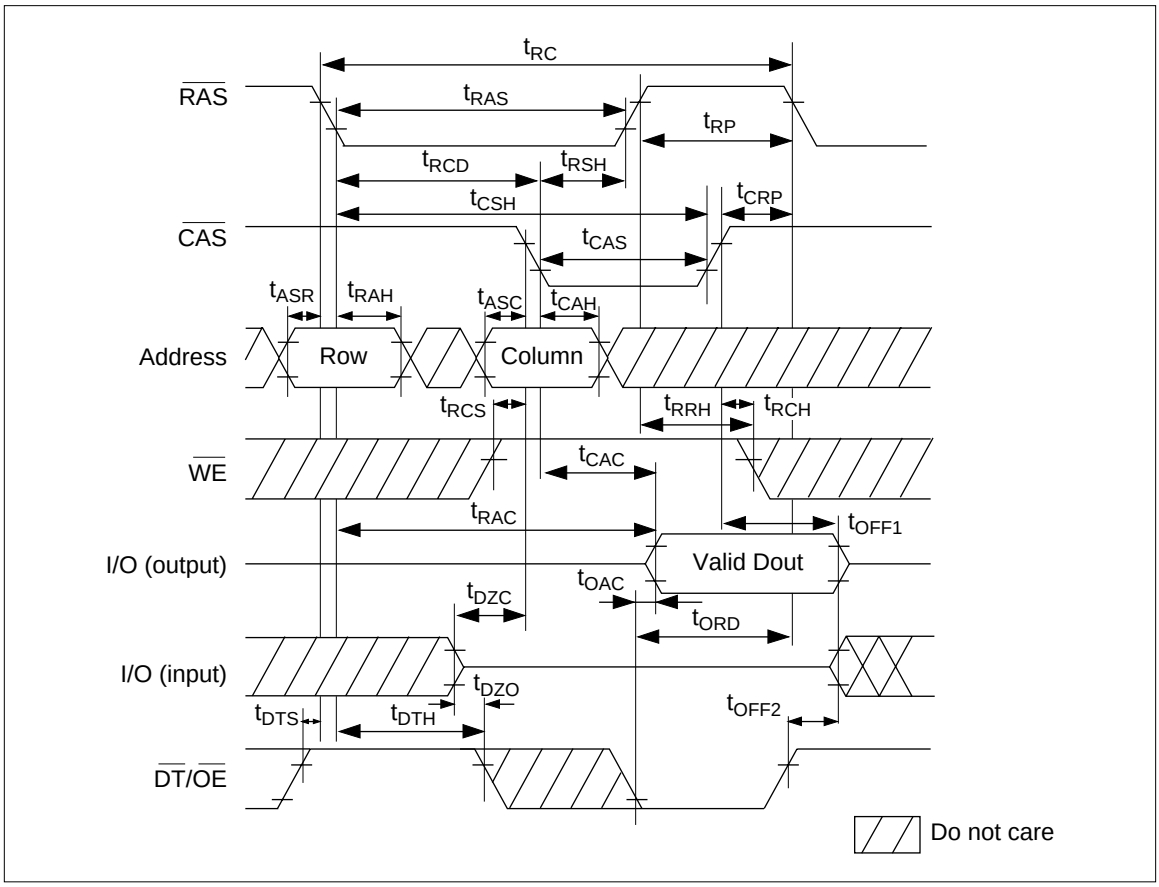
Electrical Characteristics and Recommended AC Operating Conditions (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)[*1, 10, 11] (cont)

Parameter	Symbol	HM53461-10 HM53462-10 Min	HM53461-10 HM53462-10 Max	HM53461-12 HM53462-12 Min	HM53461-12 HM53462-12 Max	HM53461-15 HM53462-15 Min	HM53461-15 HM53462-15 Max	Unit	Note
Serial write disable hold time	t_{SWIH}	35	—	35	—	55	—	ns	
$\overline{DT}$ to Sout in low-Z delay time	t_{DLZ}	5	—	10	—	10	—	ns	

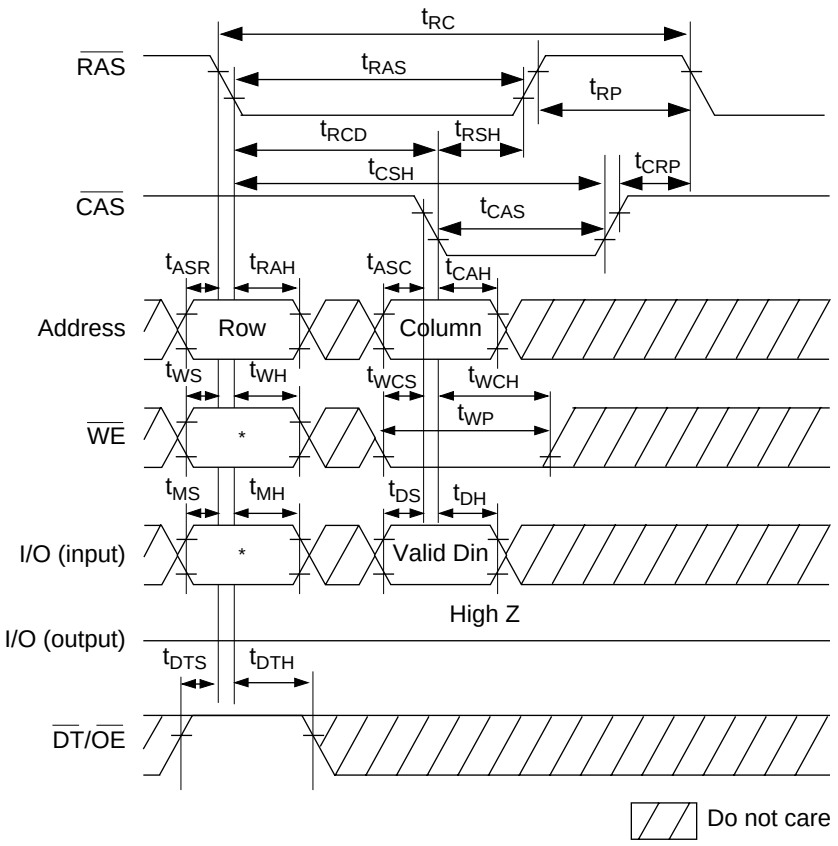
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to two TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH}(min) and V_{IL}(max) are reference levels for measuring the timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. Measured with a load circuit equivalent to two TTL and 50 pF.
11. An initial pause of 100 µs is required after power-up. Then execute at least eight initialization cycles (HM53461 Series). After power-up, pause for more than 100 µs and execute at least 8 initialization cycles. Then execute at least one logic reset cycle including write mask reset (on the falling edge of $\overline{RAS}$, $\overline{WE}$ = low and I/O1–I/O4 = high and execute one or more transport cycles for initiation of the SAM port (HM53462 Series).
12. After a read transfer cycle, the first SAM must be read out before the $\overline{CAS}$ falling edge in the succeeding read transfer cycle. When SAM is not read out after a read transfer cycle or when SAM read out is not used as valid data, the restriction mentioned above is not required.

Timing Waveforms

Read Cycle

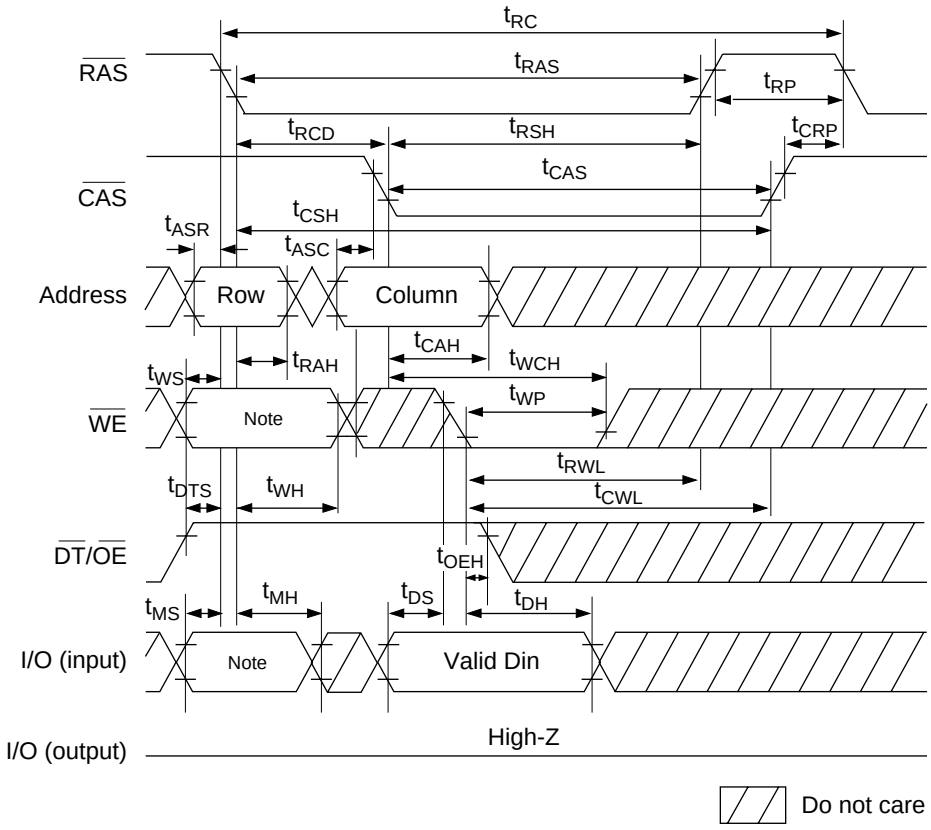


Early Write Cycle



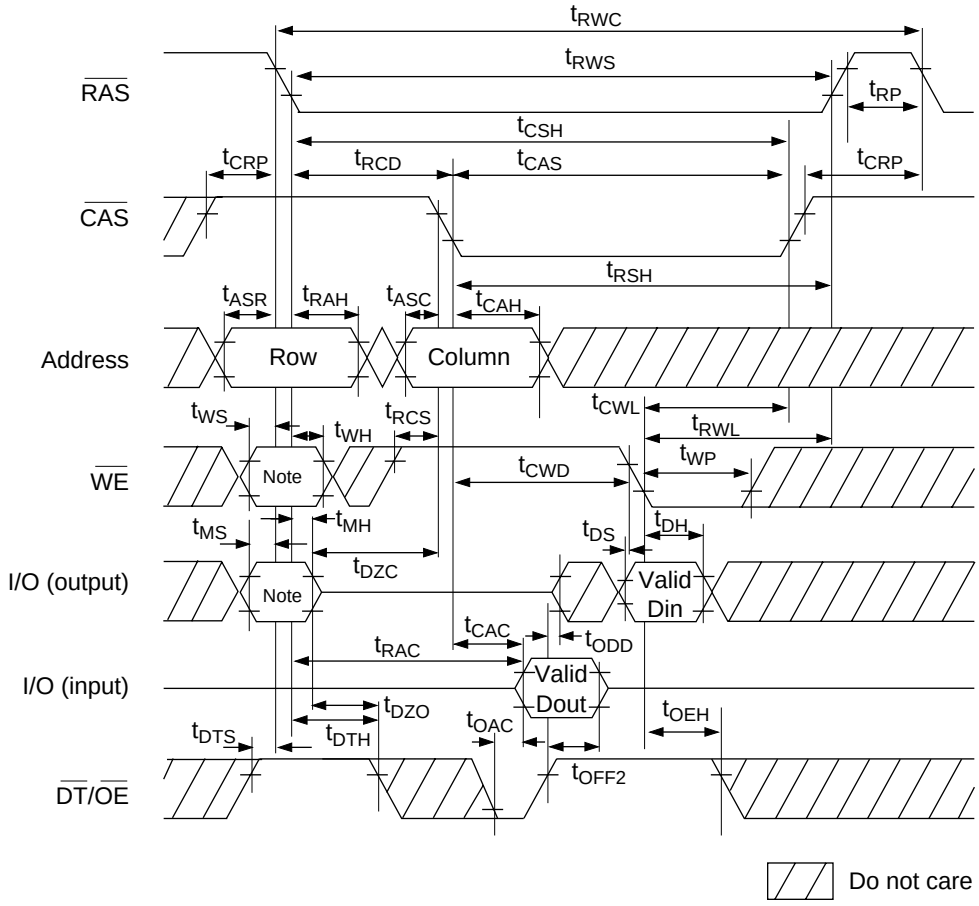
Note: When $\overline{WE}$ is high, all the data on the I/O can be written into the cell.
When $\overline{WE}$ is low, the data on the I/O are not written except when I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle



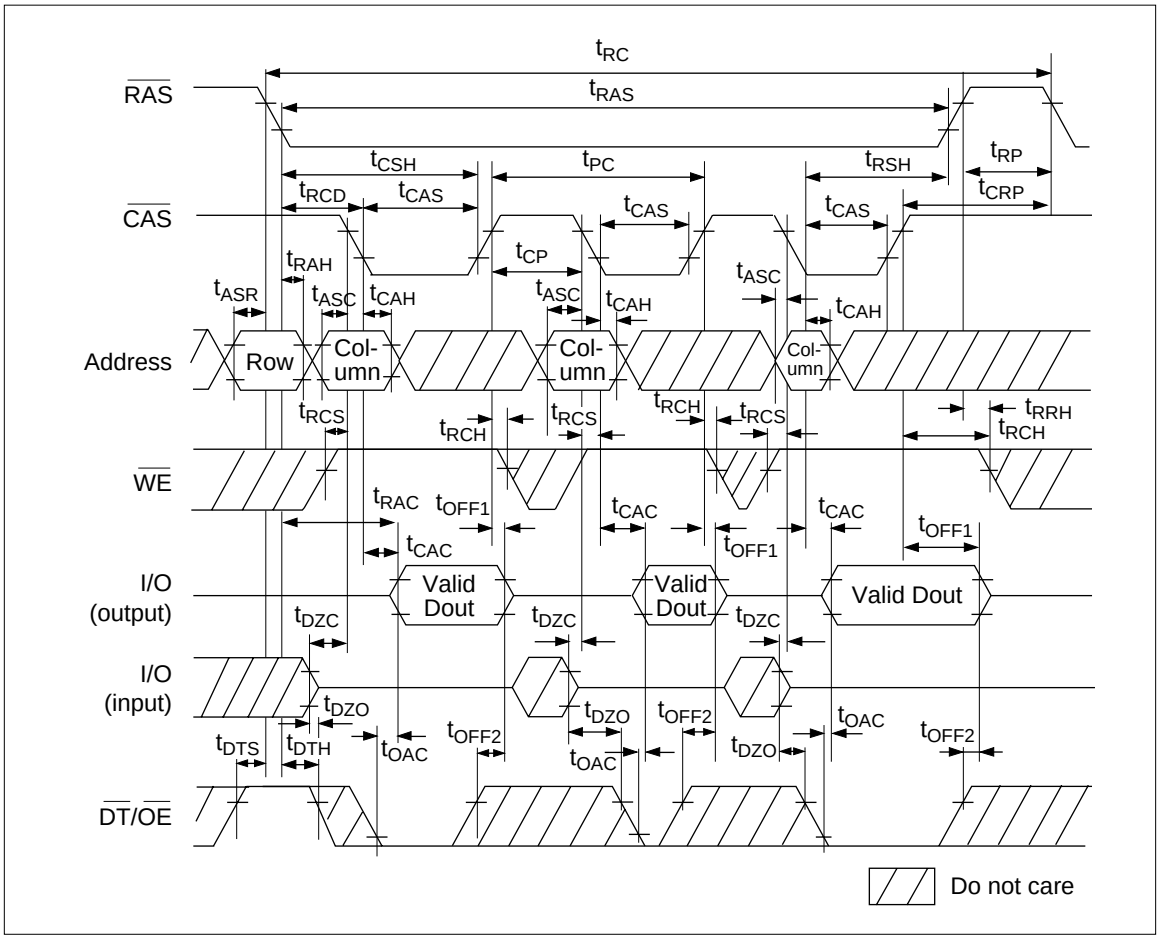
Note: When $\overline{WE}$ is high, all the data on I/O1–I/O4 can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except when I/O = high at the falling edge of $\overline{RAS}$.

Read Modify Write Cycle

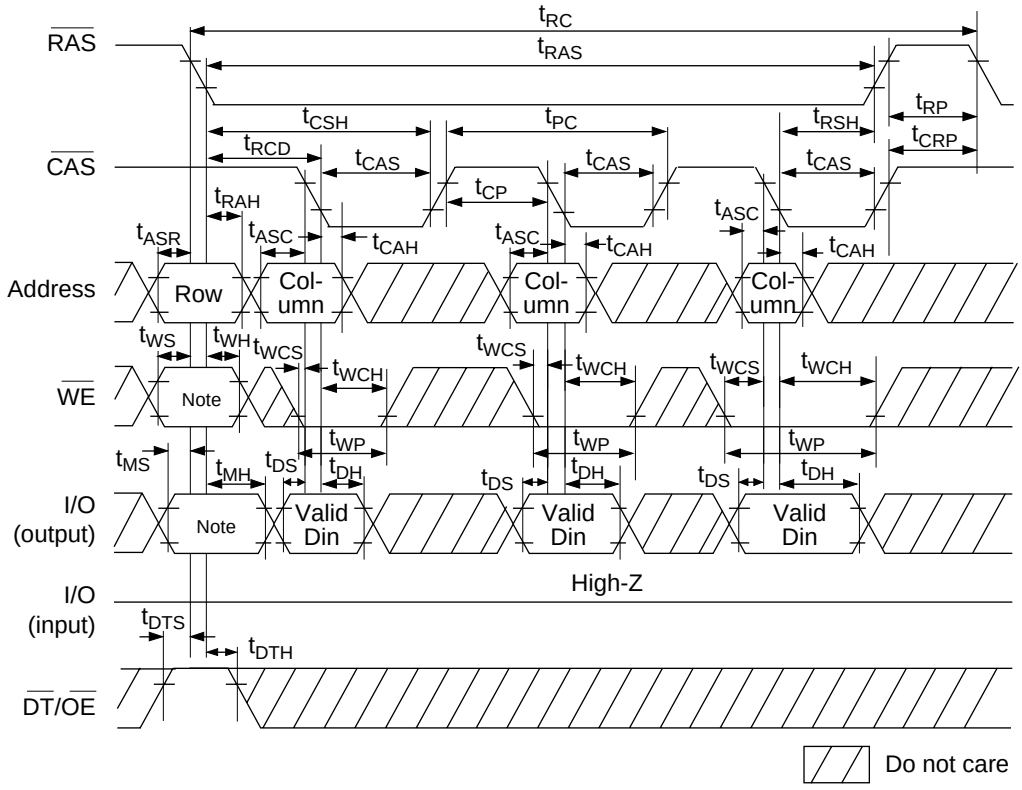


Note: When $\overline{WE}$ is high, all the data on I/O1–I/O4 can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except when I/O = high at the falling edge of $\overline{RAS}$.

Page Mode Read Cycle

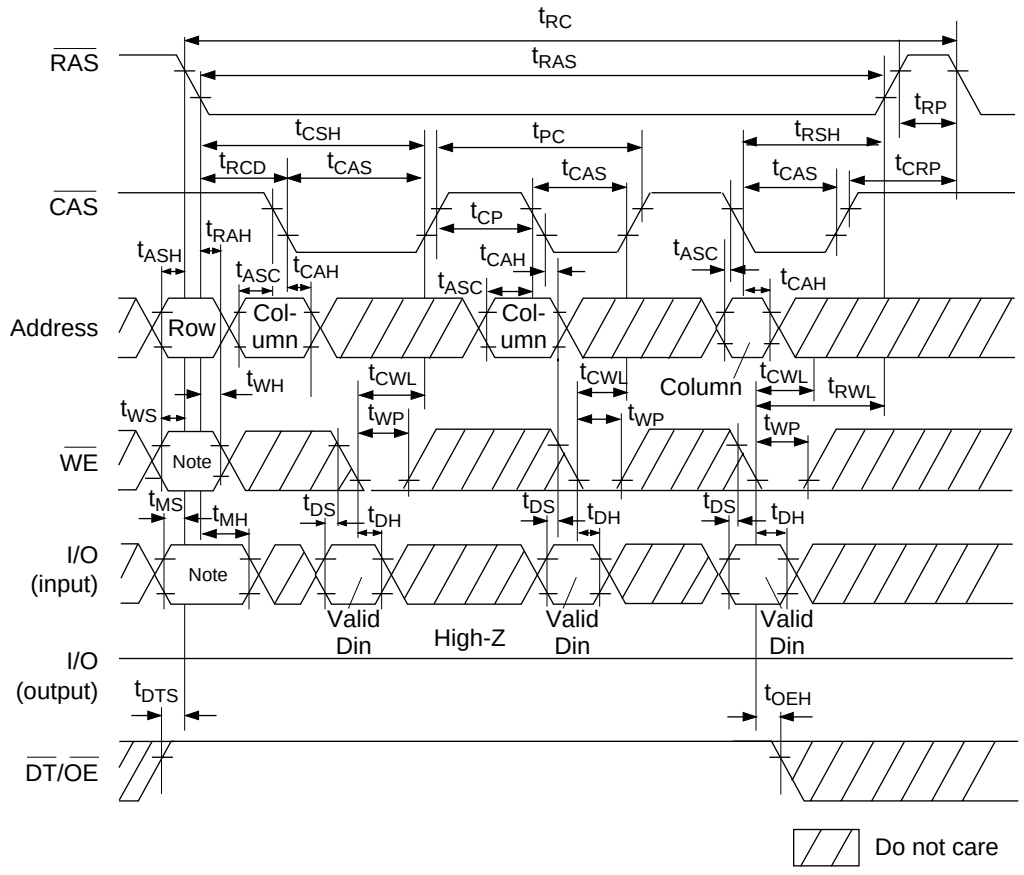


Page Mode Write Cycle (Early Write)



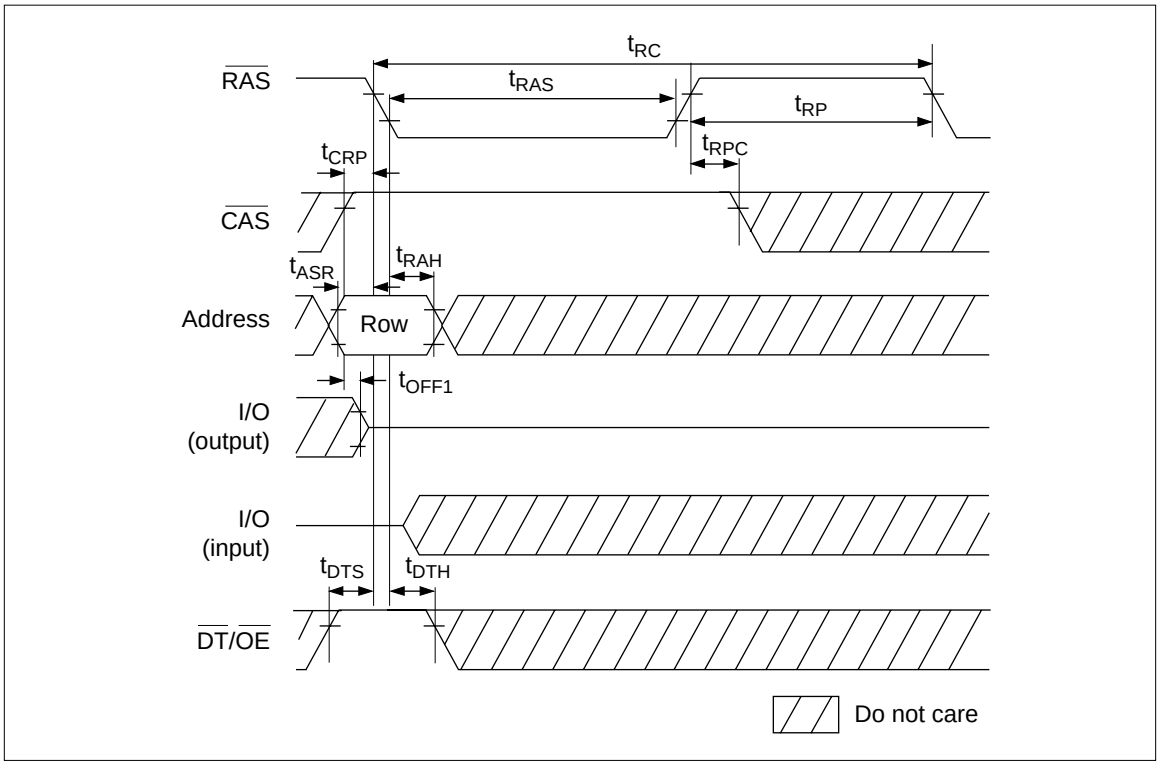
Note: When $\overline{WE}$ is high, all the data on I/O1–I/O4 can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except when I/O = high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write)

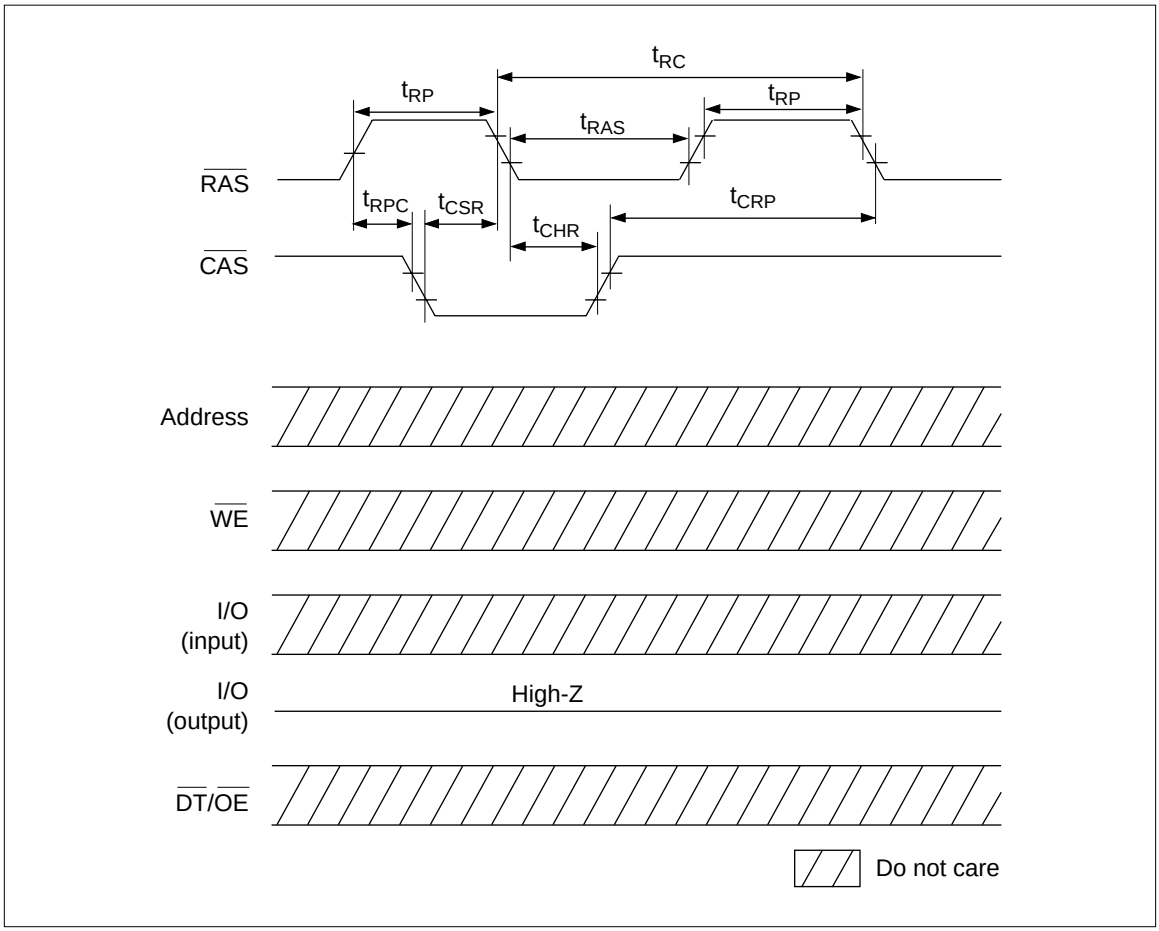


Note: When $\overline{WE}$ is high, all the data on I/O1–I/O4 can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except when I/O = high at the falling edge of $\overline{RAS}$.

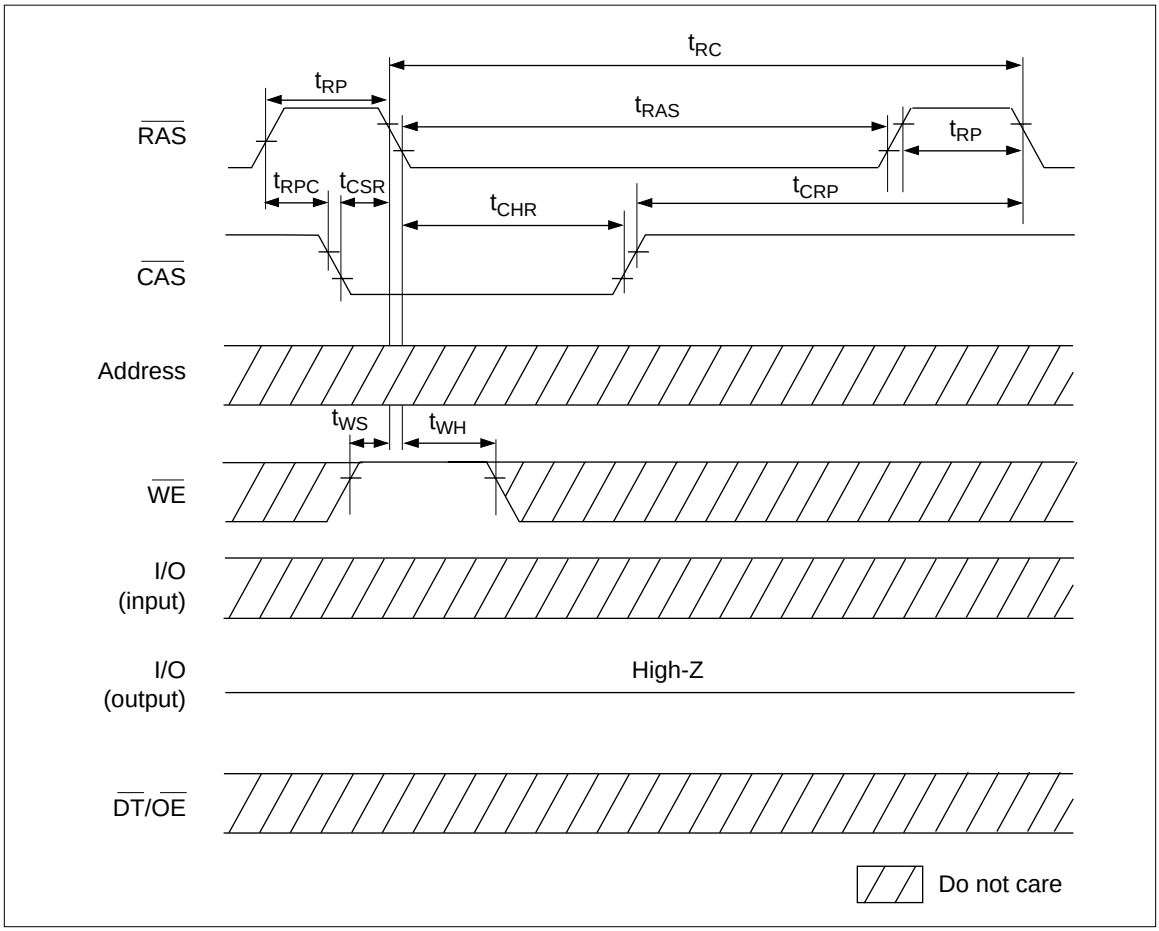
$\overline{\text{RAS}}$-Only Refresh Cycle



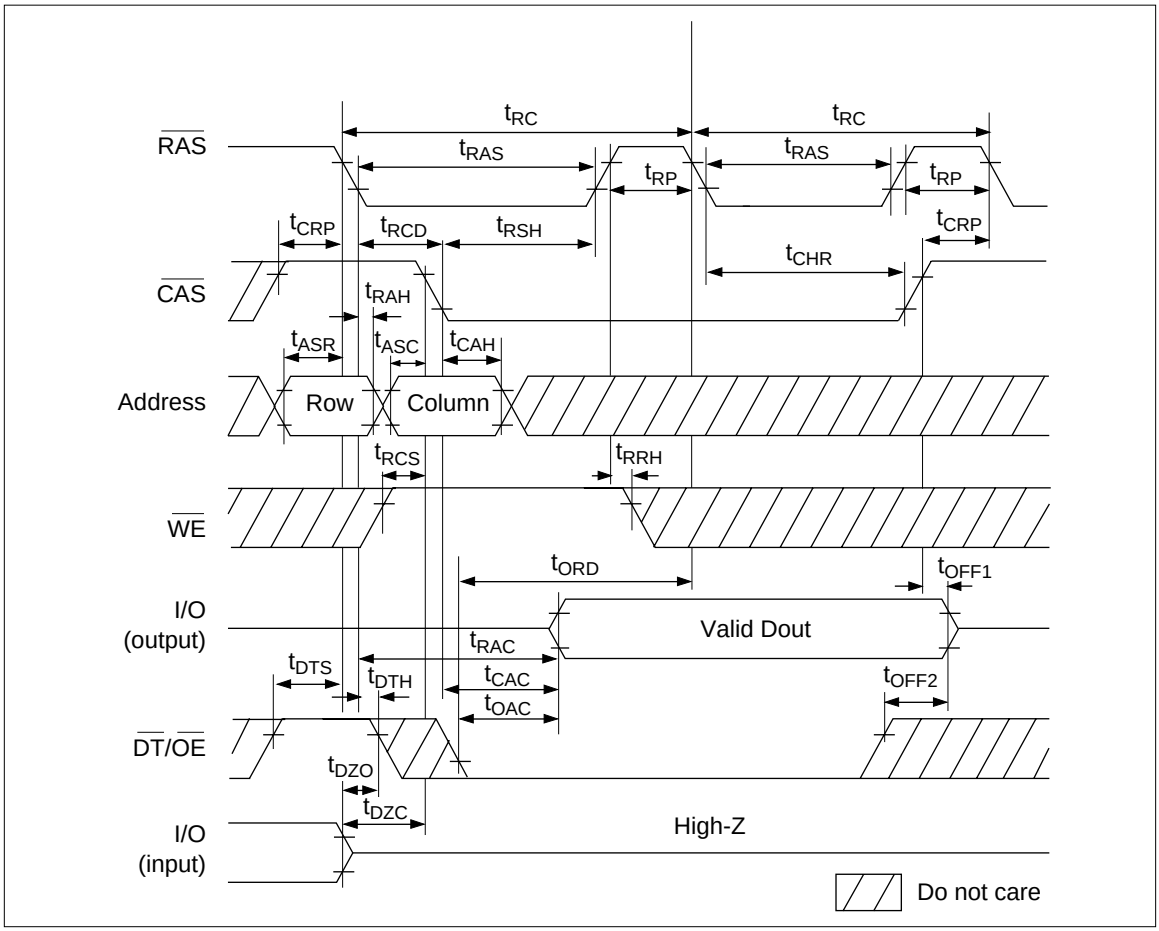
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle (HM53461 Series)



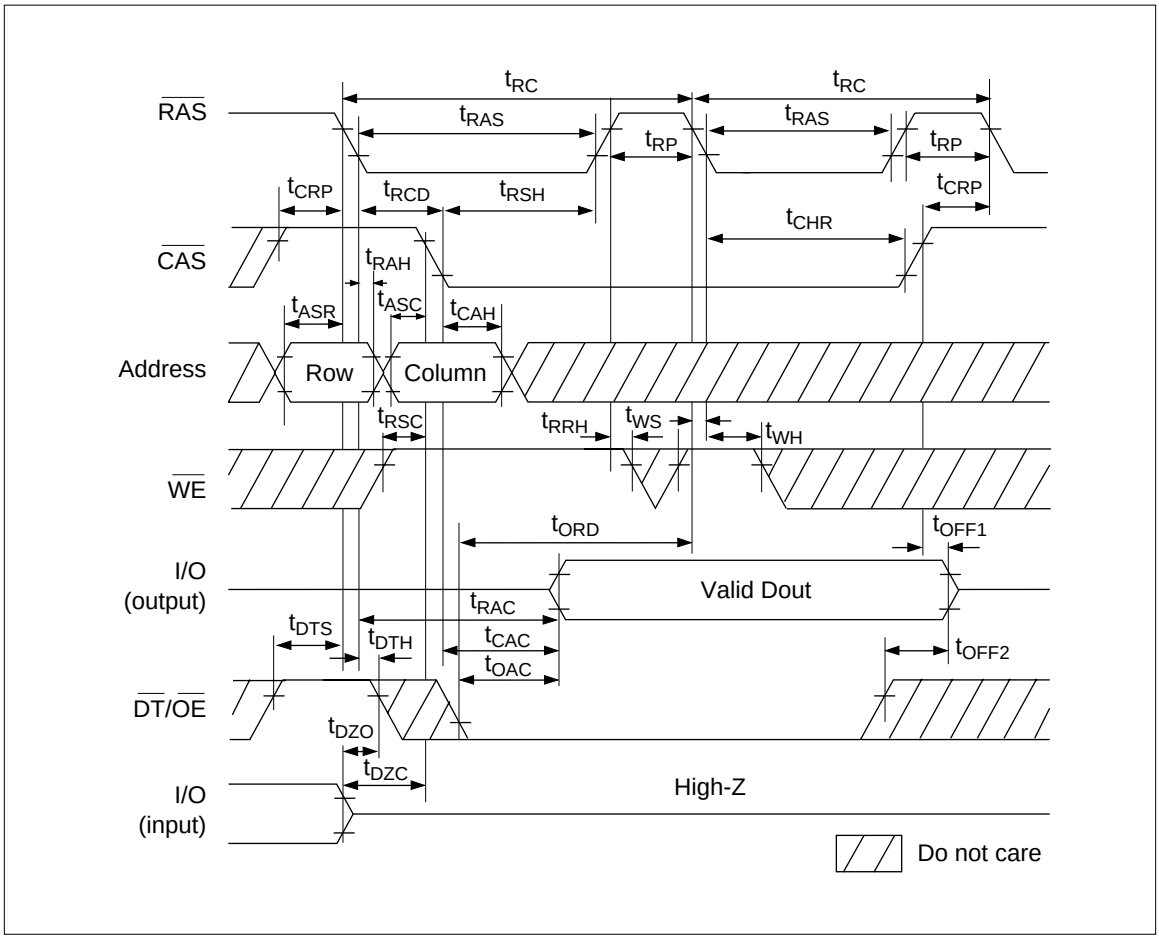
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh (HM53462 Series)



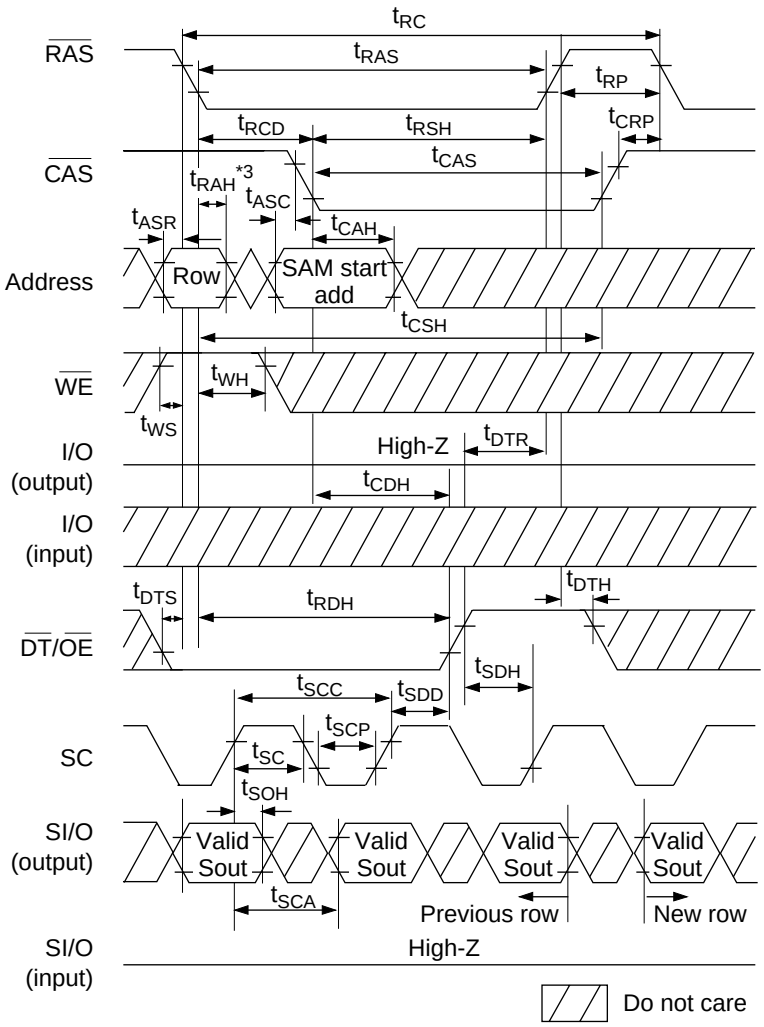
Hidden Refresh Cycle (HM53461 Series)



Hidden Refresh Cycle (HM53462 Series)

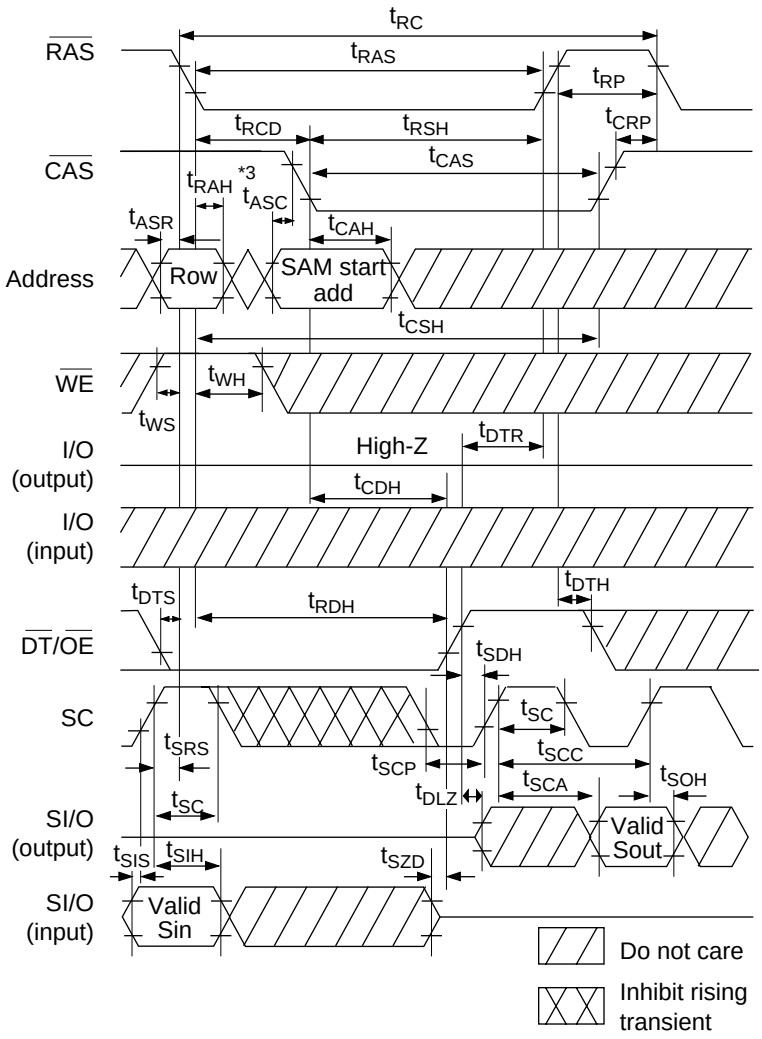


Read Transfer Cycle (1) *1, 2



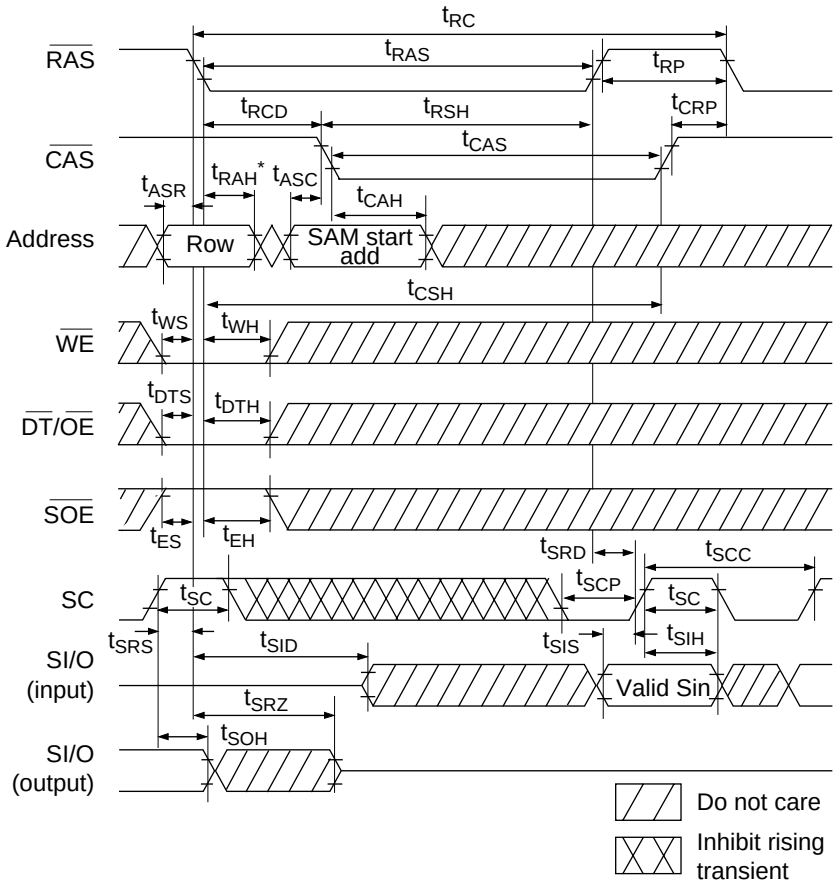
Notes: 1. In the case that the previous data transfer cycle was read transfer.
2. Assume that $\overline{SOE}$ is low.
3. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

Read Transfer Cycle (2) *1, 2



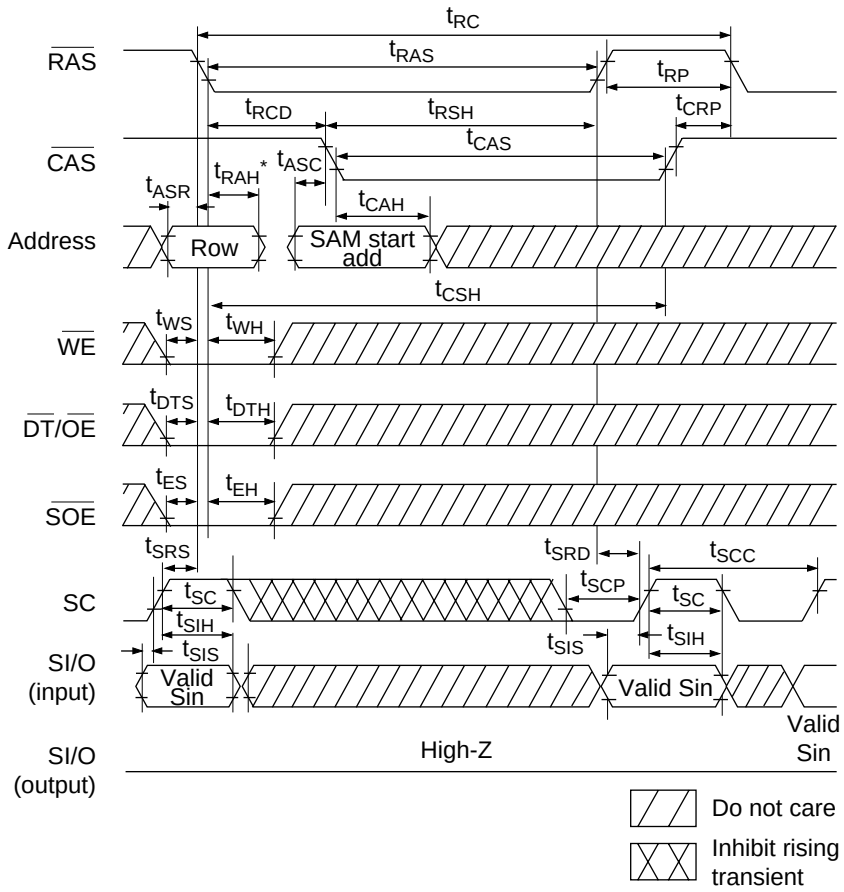
Notes: 1. In the case that the previous data transfer cycle was write transfer or pseudo transfer.
2. Assume that $\overline{SOE}$ is low.
3. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

Psuedo Transfer Cycle



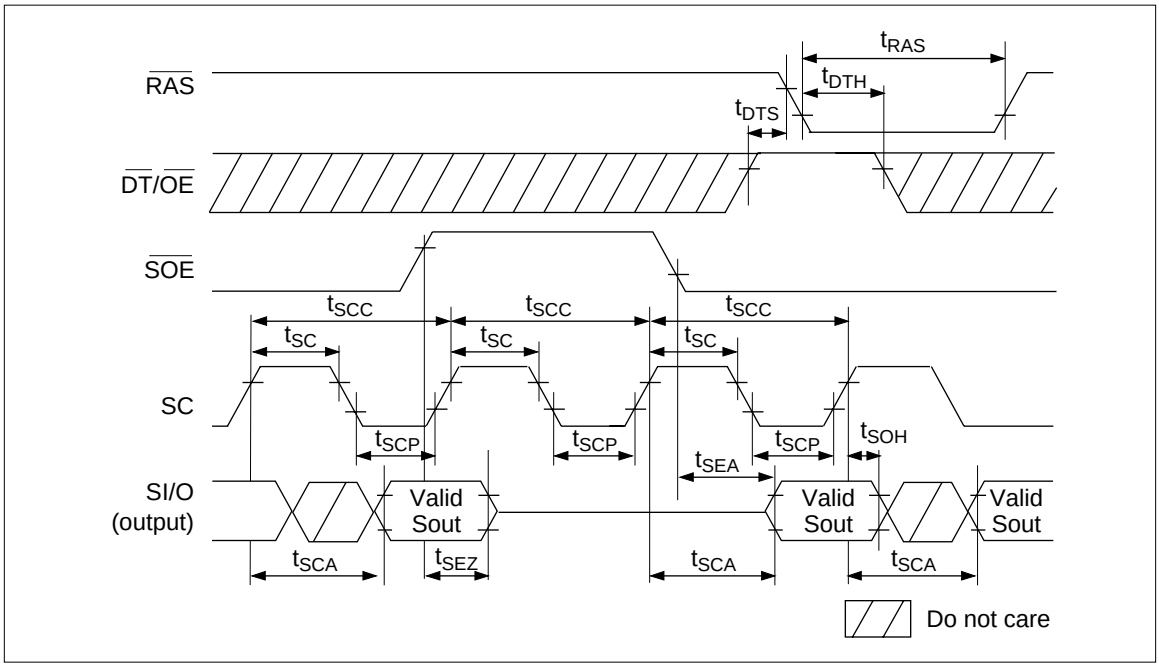
Note: $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

Write Transfer Cycle

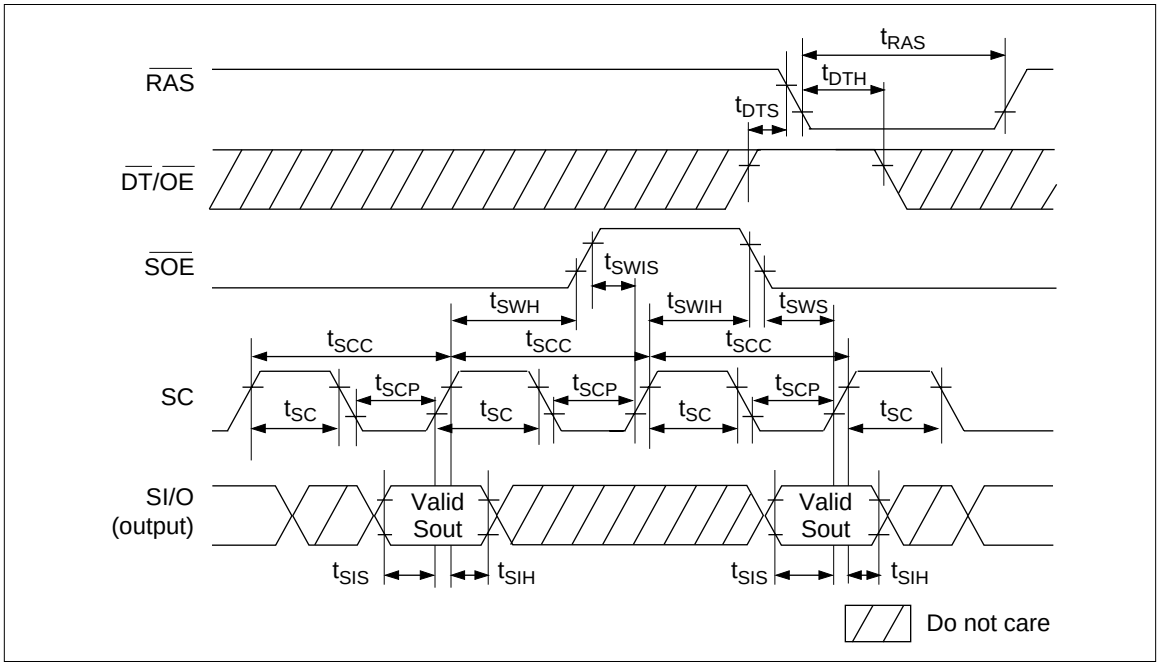


Note: $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

Serial Read Cycle



Serial Write Cycle



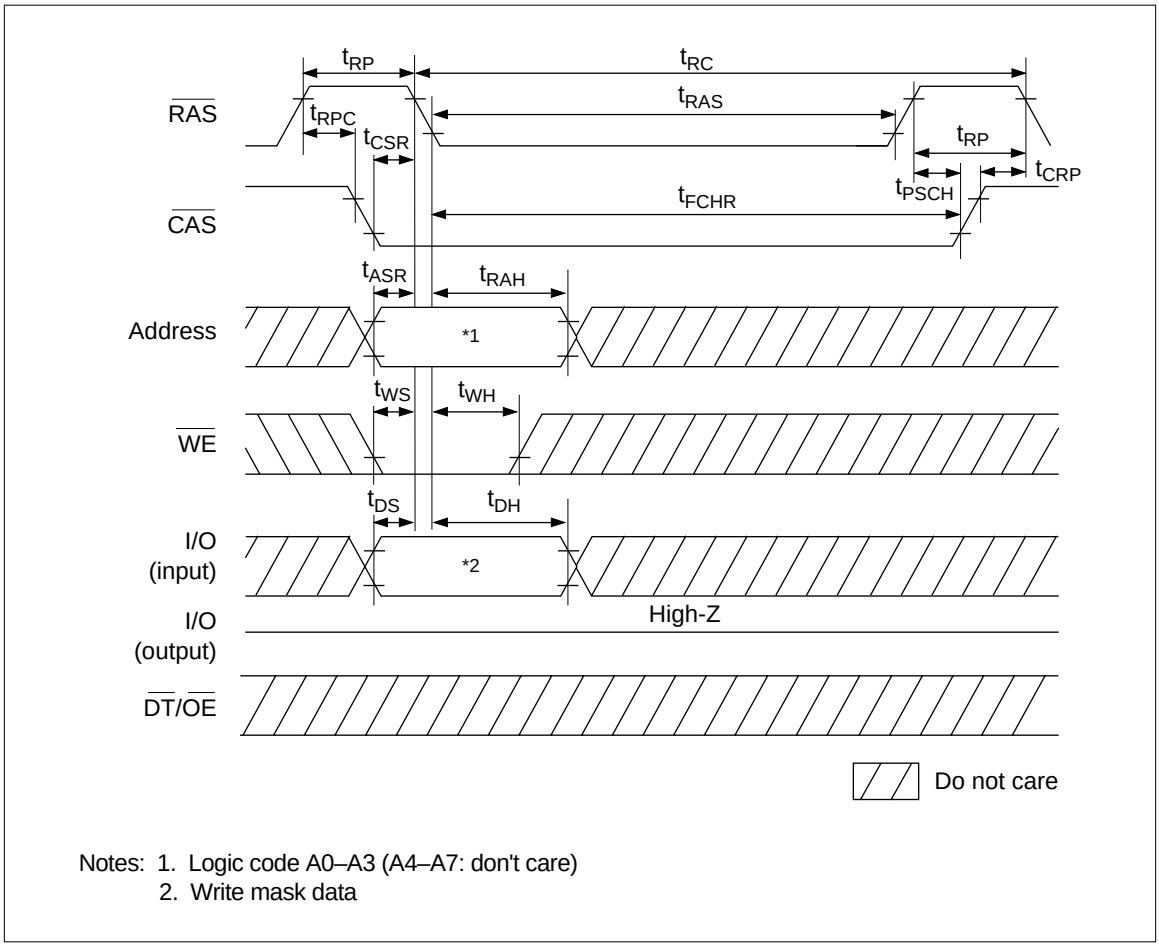
AC Characteristics (Logic operation mode) (HM53462 Series)

Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write cycle time	t_{FRC}	230	—	265	—	310	—	ns
$\overline{RAS}$ pulse width in write cycle	t_{RFS}	140	10000	165	10000	200	10000	ns
$\overline{CAS}$ pulse width in write cycle	t_{CFS}	80	10000	95	10000	105	10000	ns
$\overline{CAS}$ hold time in write cycle	t_{FCSH}	140	—	165	—	200		ns
$\overline{RAS}$ hold time in write cycle	t_{FRSH}	80	—	95	—	105	—	ns
Page mode cycle time (write cycle)	t_{FPC}	100	—	120	—	135	—	ns
$\overline{CAS}$ hold time (Logic operation set/reset cycle)	t_{FCHR}	90	—	100	—	120	—	ns
$\overline{CAS}$ hold time from $\overline{RAS}$ precharge (X4 to X1 set cycle)	t_{PSCH}	10	—	10	—	10	—	ns

Logic Code (FC0–FC3 are Ax0–Ax3 in Logic Operation Set Cycle) (HM53462 Series)

				Logic		
FC3	FC2	FC1	FC0	Symbol	Write Data	Description
0	0	0	0	0	Zero	—
0	0	0	1	AND1	Di·Mi	—
0	0	1	0	AND2	$\overline{Di}$·Mi	—
0	0	1	1	X4 to X1	—	SAM organization changes to 1024 × 1
0	1	0	0	AND3	Di·$\overline{Mi}$	—
0	1	0	1	THROUGH	Di	Logic operation mode reset
0	1	1	0	EOR	Di·Mi + Di·$\overline{Mi}$	—
0	1	1	1	OR1	Di + Mi	—
1	0	0	0	NOR	$\overline{Di}$·$\overline{Mi}$	—
1	0	0	1	ENOR	Di·Mi + $\overline{Di}$·$\overline{Mi}$	—
1	0	1	0	INV1	$\overline{Di}$	—
1	0	1	1	OR2	$\overline{Di}$ + Mi	—
1	1	0	0	INV2	$\overline{Mi}$	—
1	1	0	1	OR3	Di + $\overline{Mi}$	—
1	1	1	0	NAND	$\overline{Di}$ + $\overline{Mi}$	Di = External data-in
1	1	1	1	1	ONE	Mi = The data of the memory cell

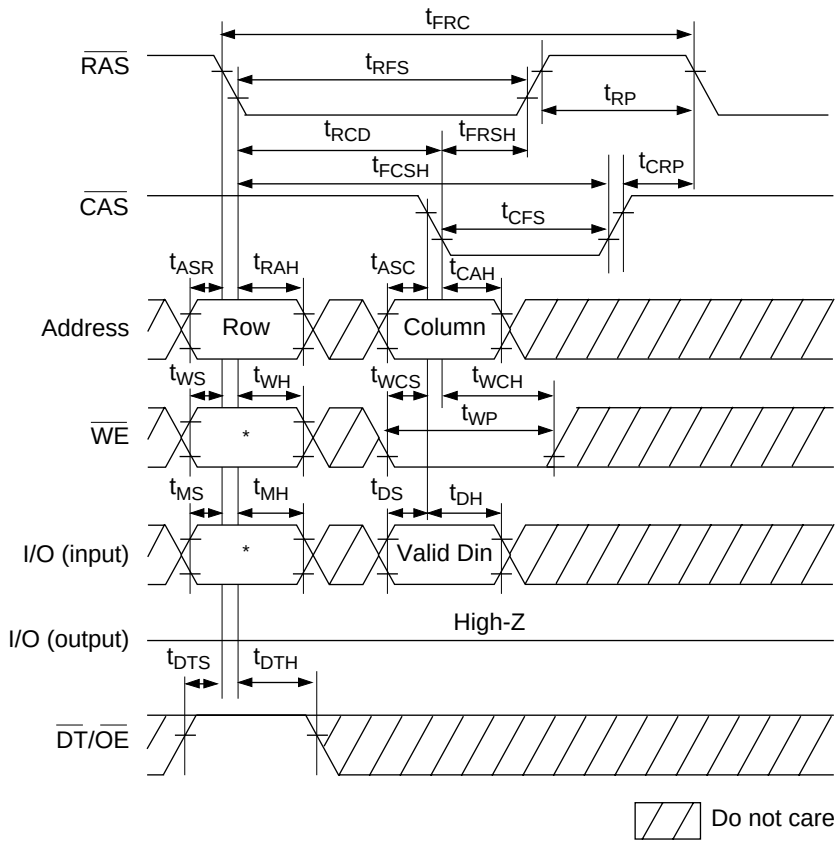
Logic Operation Set/Reset Cycle (with $\overline{CAS}$ before $\overline{RAS}$ refresh) (HM53462 Series)



Notes: 1. Logic code A0–A3 (A4–A7: don't care)
2. Write mask data

Logic Operation Mode

Early Write Cycle (HM53462 Series)



Note: When $\overline{WE}$ is high, all data on the I/O can be written into the cell. When $\overline{WE}$ is low, the data on the I/O are not written except when I/O is high at the falling edge of $\overline{RAS}$.

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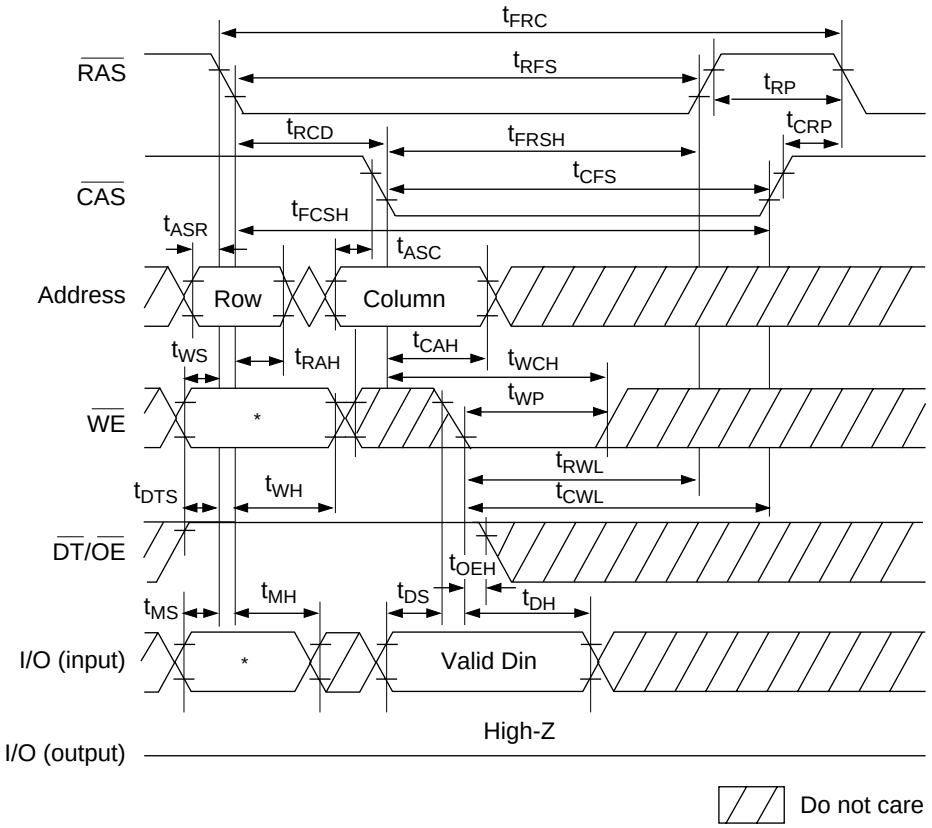
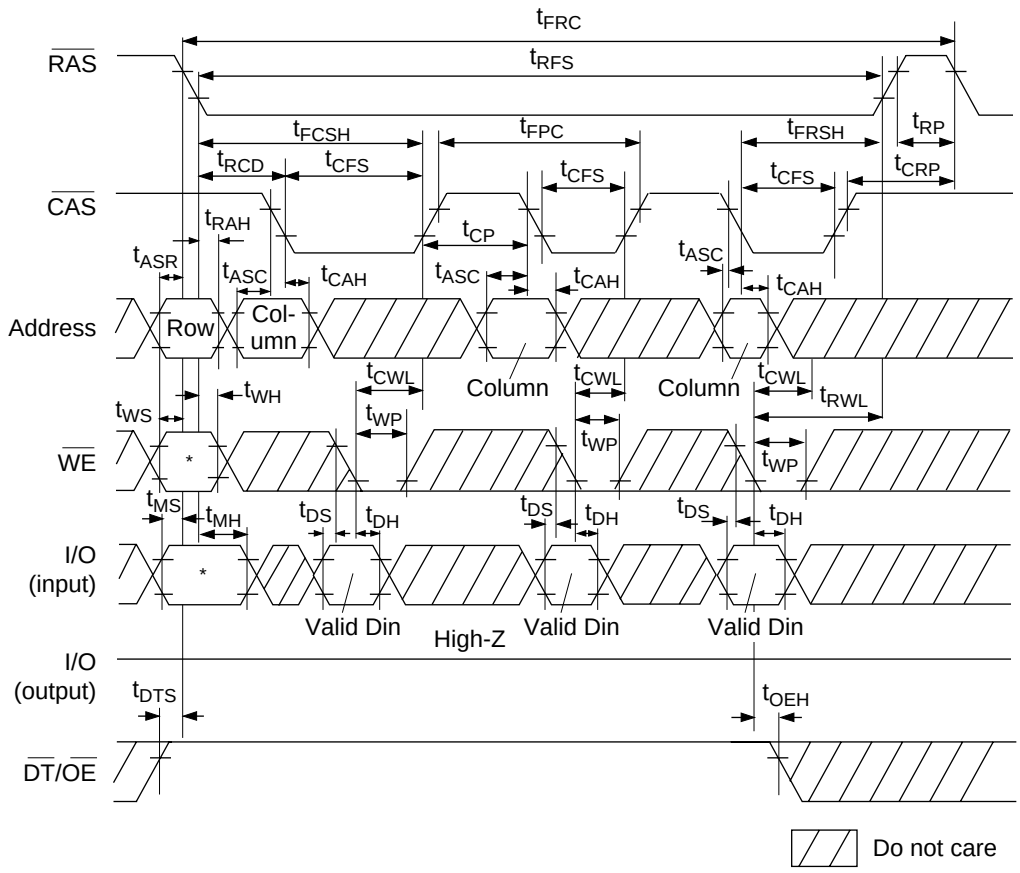
Delayed Write Cycle (HM53462 Series)



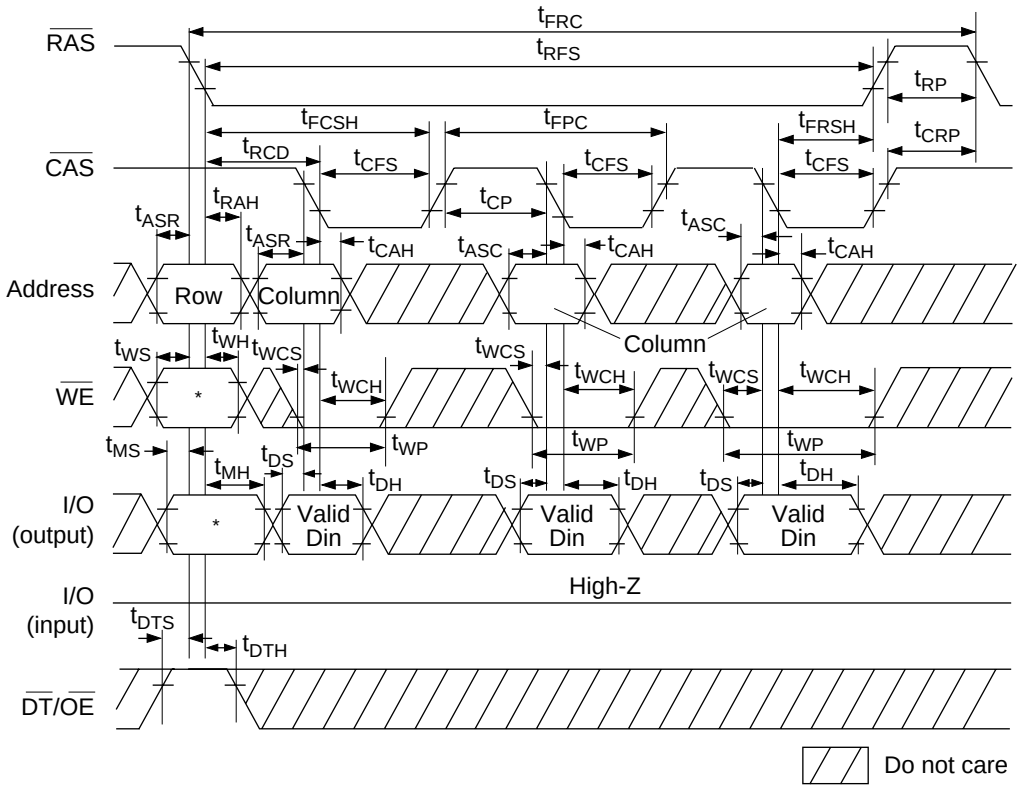
Note: When $\overline{WE}$ is high, all data on I/O1–I/O4 can be written into the memory cell. When $\overline{WE}$ is low, the data on the I/O are not written except when I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write) (HM53462 Series)



Note: When $\overline{WE}$ is high all data on the I/O can be written into the cell. When $\overline{WE}$ is low, the data on the I/O are not written except when I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Early Write) (HM53462 Series)



Note: When $\overline{WE}$ is high, all data on the I/O can be written into the cell. When $\overline{WE}$ is low, the data on the I/O are not written except when I/O is high at the falling edge of $\overline{RAS}$.

HM53462 Series Description

Logic Operation Mode

HM53462 has an internal logic operation unit which makes a process of graphics simple. The logic is determined in the logic operation set/reset cycle, and the operation is executed in every write cycle succeeding to the logic operation set/reset cycle. In this mode the internal read-modify-write operation is executed and the cell data is converted into the new data given by the logic operation between Din and the old cell data.

Logic Operation Set/Reset Cycle

A logic operation set/reset cycle is performed by bringing $\overline{CAS}$ and $\overline{WE}$ low when $\overline{RAS}$ falls (figure 1). The logic code and the bits to be masked are determined respectively by A × 0–A × 3 state and I/01–I/04 state at the falling edge of $\overline{RAS}$. Furthermore, in this cycle the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation is executed also. In the case of executing the conventional $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, $\overline{WE}$ must be high when $\overline{RAS}$ falls.

Logic Code: The logic code is shown in the following logic code table. When power is turned on, at least one logic reset cycle including write mask reset is required to initialize logic code. If the logic code is (A × 3, A × 2, A × 1, A × 0) = (0, 0, 1, 1), the SAM organization is changed converter (figure 2). In the case that the SAM organization is changed to 1,024 × 1, one data transfer cycle is needed to initialize the SAM selector.

Once the SAM organization is changed to 1024 × 1, this code is maintained unless power is turned off.

Write Mask: HM53462 has two kinds of mask registers (register 1, 2). Register 1 is set by bringing $\overline{WE}$ low at the falling edge of $\overline{RAS}$ during the write cycle, and the mask data is available only in this cycle. Register 2 is set by level of I/O in the logic operation set/reset cycle, and the mask data is available until the next logic operation set/reset cycle. If register 1 is set during the current logic operation mode, the mask data of the register is preferred (that of register 2 is ignored) and the logic becomes “THROUGH” only in this cycle (figure 3).

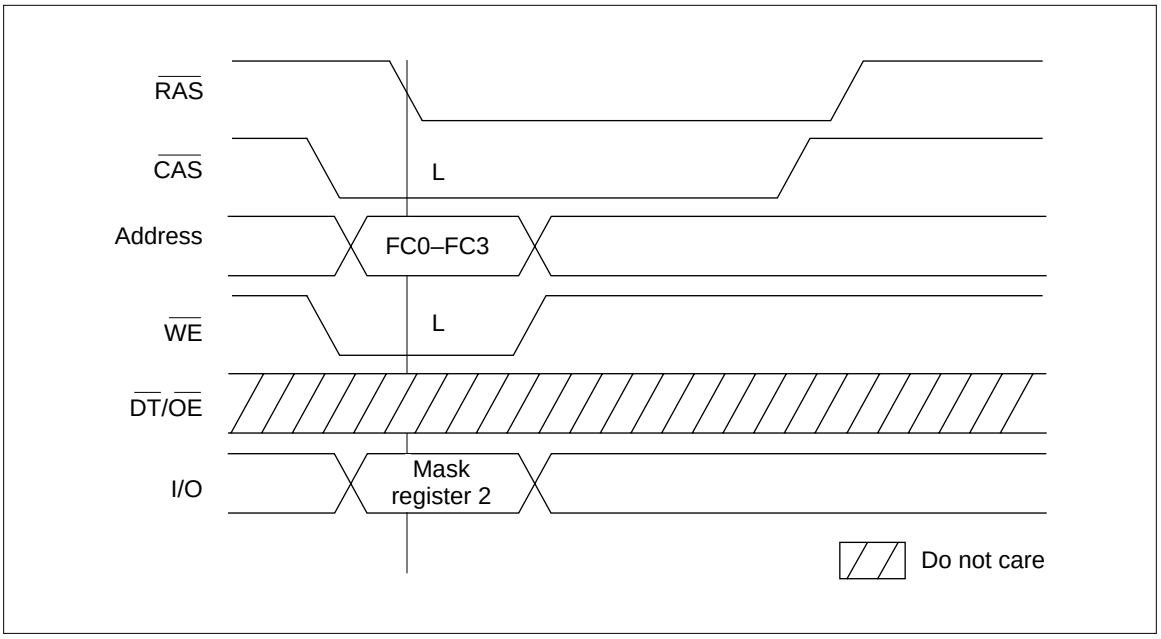


Figure 1 Logic Operation Set/Reset Cycle

Logic Code (FC0–FC3 are Ax0–Ax3 in Logic Operation Set Cycle)

				Logic		
FC3	**FC2**	**FC1**	**FC0**	**Symbol**	**Write Data**	**Description**
0	0	0	0	0	Zero	—
0	0	0	1	AND1	Di·Mi	—
0	0	1	0	AND2	$\overline{Di}$·Mi	—
0	0	1	1	X4 to X1	—	SAM organization changes to 1024 × 1
0	1	0	0	AND3	Di·$\overline{Mi}$	—
0	1	0	1	THROUGH	Di	Logic operation mode reset
0	1	1	0	EOR	$\overline{Di}$·Mi + Di·$\overline{Mi}$	—
0	1	1	1	OR1	Di + Mi	—
1	0	0	0	NOR	$\overline{Di}$·$\overline{Mi}$	—
1	0	0	1	ENOR	Di·Mi + $\overline{Di}$·$\overline{Mi}$	—
1	0	1	0	INV1	$\overline{Di}$	—
1	0	1	1	OR2	$\overline{Di}$ + Mi	—

Logic Code (FC0–FC3 are Ax0–Ax3 in Logic Operation Set Cycle) (cont)

				Logic		
FC3	**FC2**	**FC1**	**FC0**	**Symbol**	**Write Data**	**Description**
1	1	0	0	INV2	$\overline{Mi}$	—
1	1	0	1	OR3	Di + $\overline{Mi}$	—
1	1	1	0	NAND	$\overline{Di}$ + $\overline{Mi}$	Di = External data-in
1	1	1	1	1	ONE	Mi = The data of the memory cell

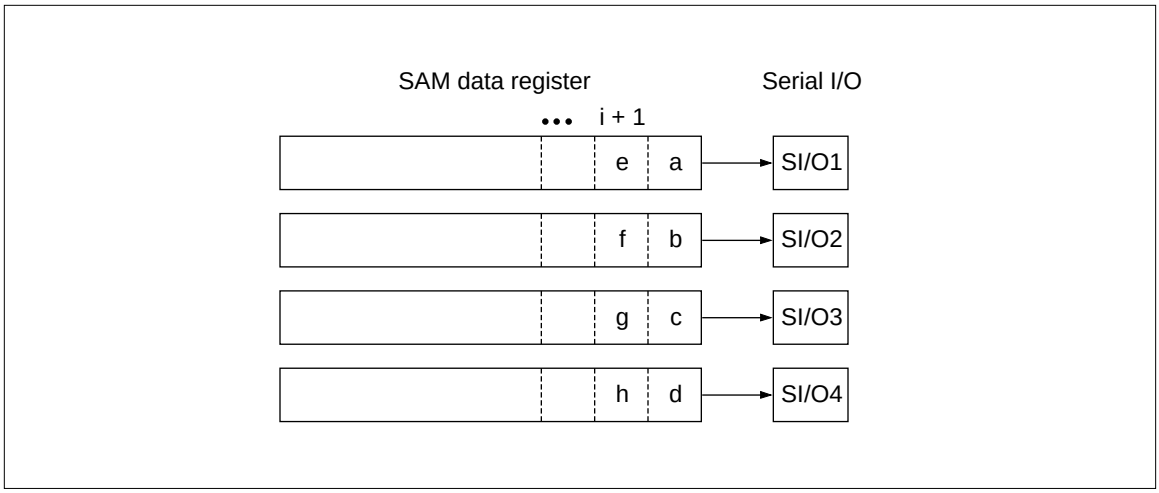
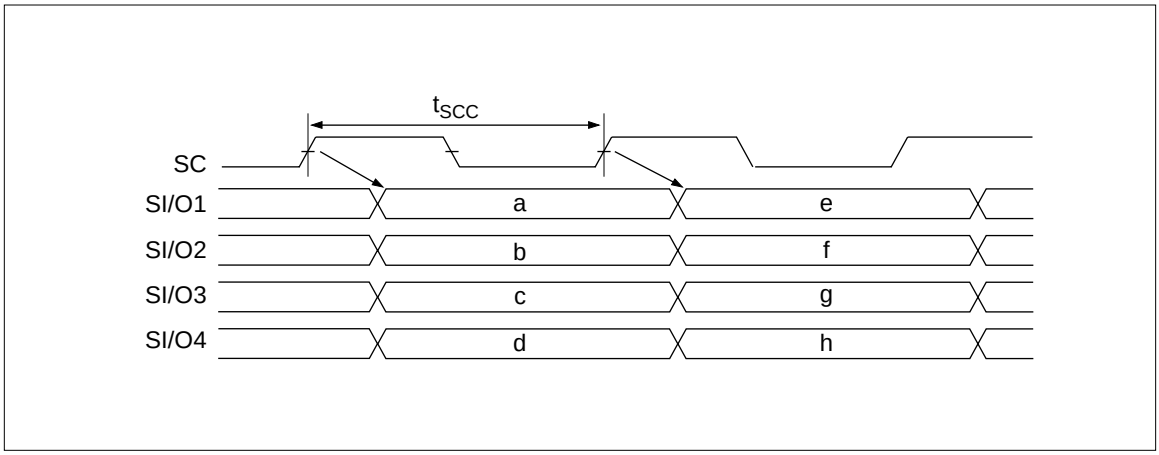


Figure 2 Shift Method of SAM Data

By-4 Mode (SAM Organization: 256 × 4)



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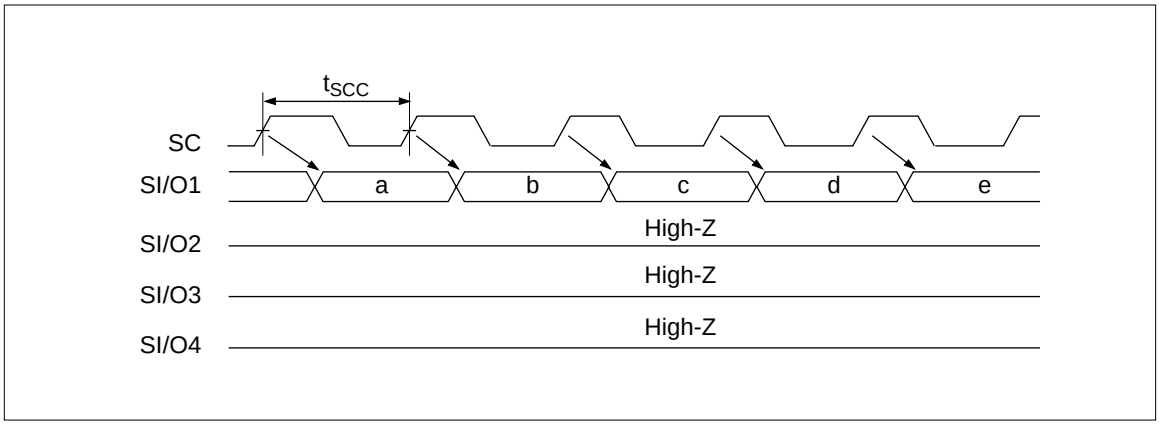
By-1 Mode (SAM Organization: 1024 × 1)



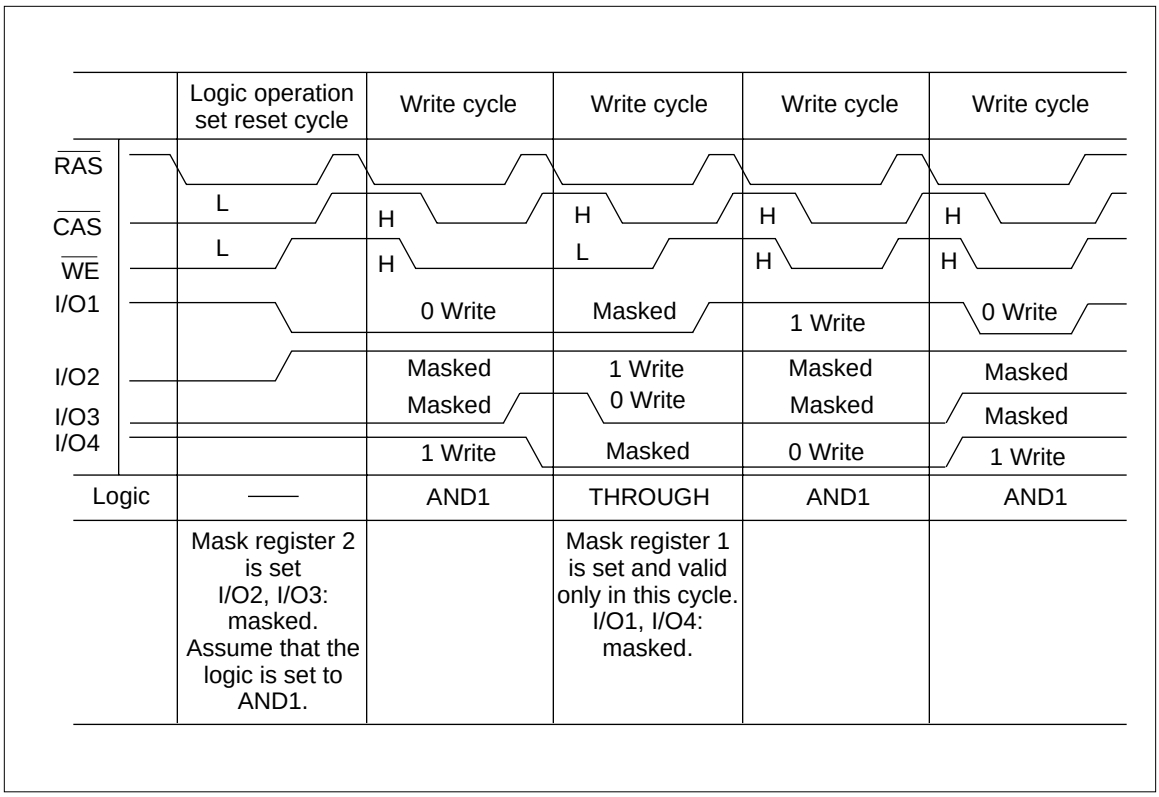


Figure 3 Example of Logic Operation Mode